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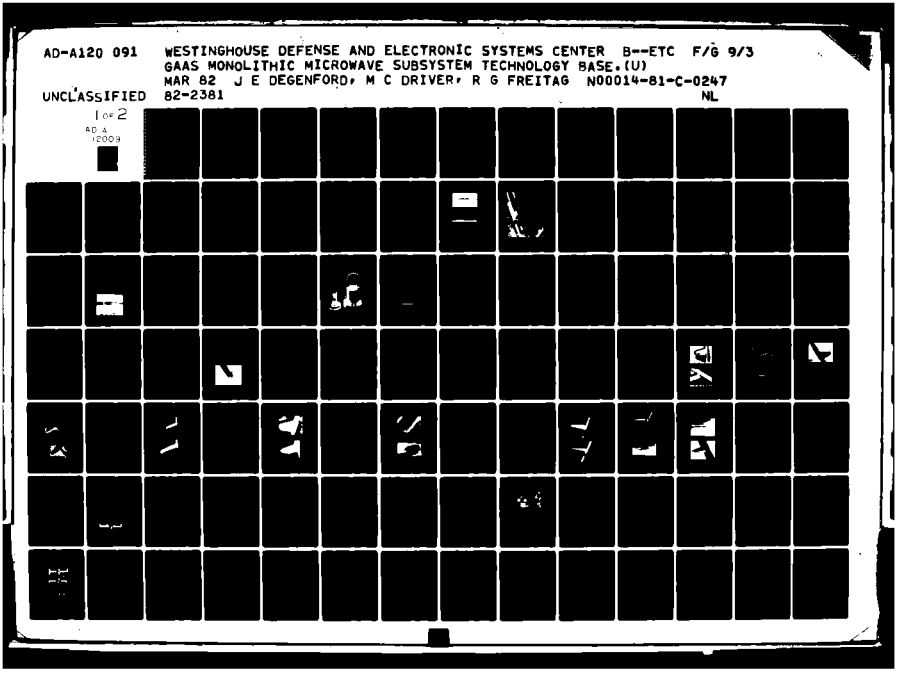

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GaAs MONOLITHIC MICROWAVE SUBSYSTEM TECHNOLOGY BASE

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During this reporting period, the effort was primarily aimed at developing a number of technologies critical to the development of a 3-W, 8-12 GHz amplifier. These technologies included 1) vias, 2) air bridges, 3) deep UV photolithography for 0.7 μm gates, 4) overlay capacitors.

In the circuit area, "cell cluster" matching techniques were demonstrated in a hybrid combiner circuit and several monolithic two-stage amplifier were evaluated. A 5-10 GHz amplifier run incorporating vias and airbridges,

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20. ABSTRACT (Continued)

was measured and produced 1 watt output from ≈5.5-9.0 GHz with 9 dB associated gain. An 8-12 GHz, two-stage amplifier was also designed using 1 micrometer gate length FETs. While these FETs were not optimum for 12-GHz operation, this amplifier was predicted and measured to have a power output of 400-500 mW with 7 dB associated gain over the 8-12 GHz range.

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1. INTRODUCTION AND SUMMARY

This report details the progress made during the first year on the program entitled "GaAs Monolithic Subsystem Technology Base" (N00014-81-C-0247). The phase II program goals - to "develop a 4 stage, 3W, 8-12 GHz monolithic amplifier" - represent a significant increase in difficulty as compared to the 1W, 5-10GHz amplifiers developed during a prior program (N00014-78-C-0268). Hence, at the start of the current program, a number of technologies critical to the development of a 3W, 8-12 GHz monolithic amplifier were identified. These technologies and a brief description of their current status are outlined in the table below:

Technology Base

Critical Technologies	Status (12 /5/81)
Vias	Complete, in amplifiers
Air Bridges	Complete, in amplifiers
Deep UV Photolithography	1. Demonstrated submicron opening in photoresist 2.Processed one run with submicron gates 3. Started 2 layer resist technology development
Overlay Capacitors	1. Chosen dielectric 2. Demonstrated air-bridge to capacitor 3. Outline processing to integrate into ICs 4. First two stage amplifier run with overlays in processing

Critical Technologies	Status (12 /5/81)
Discrete FETs	Demonstrated 0.3-0.4 W/mm at 12GHz for 0.7 micron gate devices
Automatic Thinning Jig	+0.00025" Uniformity in amplifier substrate thickness over 2" diameter.
Cluster Matching for 3W FET	1. Developed resonant floating node for improved isolation 2. Verified cluster matching concept with hybrid combiner and achieved 1.8 watt output 3. Developed implanted resistors for isolation network

Note that in the process technology area, the development of vias and air bridges is complete and routinely being included in amplifier runs, while a run of two stage amplifiers employing overlay capacitors is underway and scheduled for completion early in 1982. A single layer resist Deep UV technology was developed and used to process a run of 0.7-micron gate length discrete FETs which yielded 0.3-0.4 W/mm power output at 12 GHz. This run included both parallel and π gate FETs and tests are continuing to ascertain if there is a clear superiority of either type at 12 GHz. A two-layer resist process is under development to improve the gate metal lift-off process yield.

In the circuit area, the concept of cell cluster matching in conjunction with a "resonant floating node" for improved isolation between cell clusters was verified in a hybrid MIC format. A hybrid combiner circuit was used to combine the power outputs of four 1200 μm (1/2 watt) FETs to produce a power output of 1.8 Watts. Studies of feedback and active matching techniques were also performed to assess their applicability to the final four-stage design. Feedback, in particular, looks very promising for the earlier low power amplifier stages of the four-stage amplifier.

The 3W, totally monolithic output stage has been designed, the implant masks have been made, and material has been implanted. Final circuit masks will be made after modelling of the 0.7 micron FETs is complete.

Several two-stage amplifier designs were also evaluated this year. A 5-10 GHz amplifier run incorporating vias and airbridges, which was in processing

at the completion of the earlier referenced program, was measured and produced 1 watt output from about 5.5-9.0 GHz with 9 dB associated gain. An 8-12 GHz two-stage amplifier was also designed using the earlier 1-micron gate length FETs. While these FETs were not optimum for 12 GHz operation, this amplifier was predicted and measured to have a power output of 400-500 mW with 7 dB associated gain over the 8-12 GHz range.

2. DEVICE FABRICATION

2.1 INTRODUCTION

At the completion of an earlier program [1] for the development of two-stage amplifiers, the technology for the etching of vias was mentioned, but not fully described. This report describes in detail the fabrication steps employed and includes the technology for the fabrication of air bridges as interconnections between the transistor sources and the vias.

The design of multistage amplifiers requires the implementation of overlay capacitors which can be made in the higher capacitance values (>2 pF) necessary for flexibility of circuit design, for matching to larger periphery power FETs, and for realizing on-chip RF bypass capacitors. Previously fabricated interdigitated capacitors are replaced by the overlay capacitors. The choice of dielectric and the fabrication procedures for these overlay capacitors are described together with the circuit design of a two-stage, 1-watt amplifier and a 3-Watt output stage using these devices.

2.2 FABRICATION TECHNOLOGIES

2.2.1 Via Fabrication

In order to ensure low source inductance and permit the grounding of components in the monolithic circuit, connections to the ground plane formed on the back of the wafer are required and are known as vias. Since the report on Phase I of this program[1], the technique for the fabrication of these vias has been improved so that the yield of complete vias on a processed wafer is better than 99 percent with observed defects as low as one incomplete via out of 270. The via fabrication technique is described in the next paragraph.

Following the completion of the GaAs power FETs and the thick-metal circuit, but before the air bridge formation, the GaAs wafer is lapped to 100 μm thickness while waxed to a glass carrier. An IR mask aligner is then used to open 50- μm squares in AZ1350 photoresist on the backside of the wafer. These holes are aligned below 250 x 250 μm metal squares on the front surface where the FETs or the microwave circuits need a ground contact (see figure 2-1a). An acid-peroxide etch is used to remove the GaAs leaving a

smooth-walled hole with tapered sides. The 250 μm square on the front surface is large enough to allow substantial leeway in the etching process across the wafer. It is also important that the metal square on the top surface not be formed under the ohmic contact metallization, as drastic lateral etching along the surface of the wafer under the ohmic metal will occur. This lateral etching reduces the yield of the via process by etching into the active area of the FETs. After etching, the wafer appears as shown in figure 2-1b. 500Å of chromium and 10,000Å of gold are then sputter-deposited on the etched back surface as shown in figure 2-1c followed by an evaporation of 800Å of chromium, 10,000Å of gold, 500Å of nickel (as a barrier) and 2000Å of gold (see figure 2-1d). The wafer is then removed from the glass slide with a thick bottom metal connecting to specific top metal sites through the via holes.

2.2.2 Air Bridge Technology

The fabrication of large periphery (2400 μm) transistors for power amplification requires the interconnection of multiple (up to nine) source areas by low inductance leads. Previous experiments have shown that via connections from each source pad to the ground plane on the back of the wafer cause problems with increased output capocitance parasitics so that in the present design, vias are formed for every 1200 μm of periphery leaving 3 source pads that must be interconnected to the via grounds. A high yield air bridge technology has been developed to effect this interconnection in a monolithic manner on 2-in. diameter wafers.

Air bridges are formed at a late stage in the device fabrication sequence after thinning of the wafer and the etching and metallization of the via contacts. AZ1375 photoresist is first spun onto the wafer at 2500 rpm to produce a layer 4.5 μm thick. The photoresist is then patterned using conventional photolithographic techniques of exposure and development. The photoresist is then baked for 10 min. This post-bake is very important, for it must harden the resist enough to form the "spacer" for the air bridge, but it must not be too difficult to remove once the air bridge is completed.

At this point, 500Å of titanium and 500Å of gold are evaporated onto the wafer to form the structure shown in figure 2-2b. A second layer of AZ1375 photoresist is then spun onto the wafer to the same thickness. It is put on rapidly so that the solvents in the resist do not attack the resist under the titanium-gold layer through pinholes in the metal.

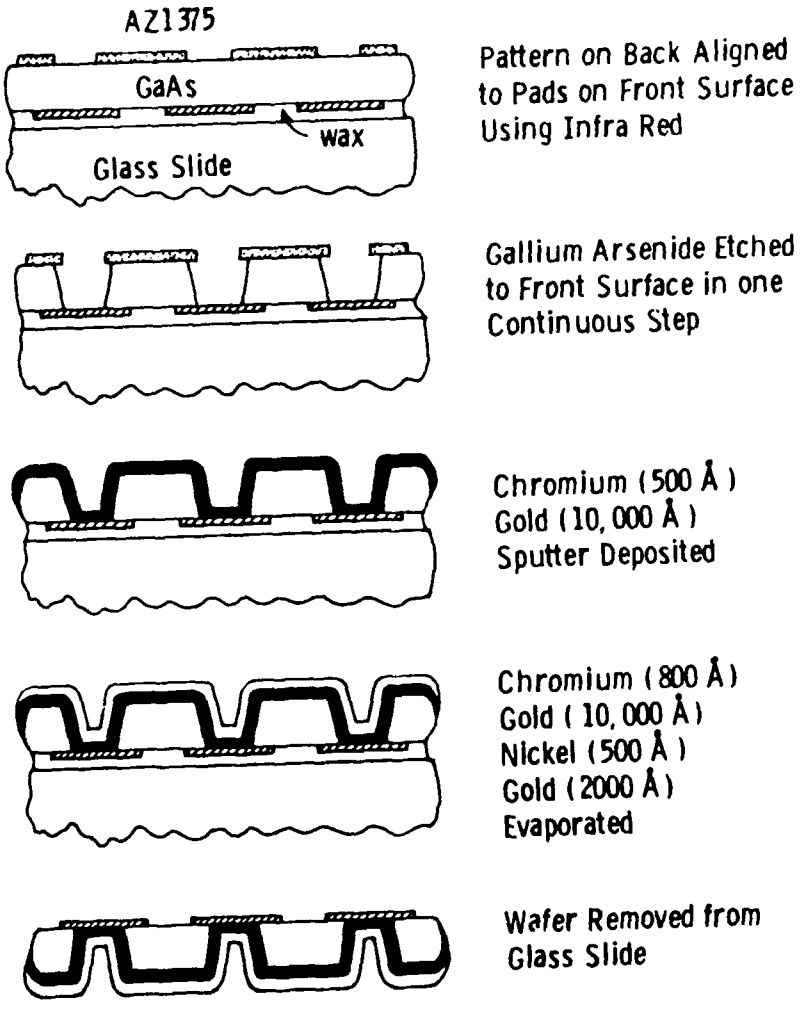
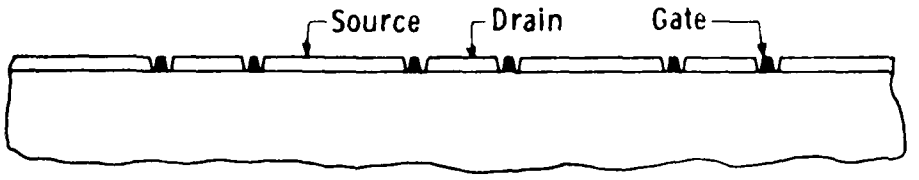
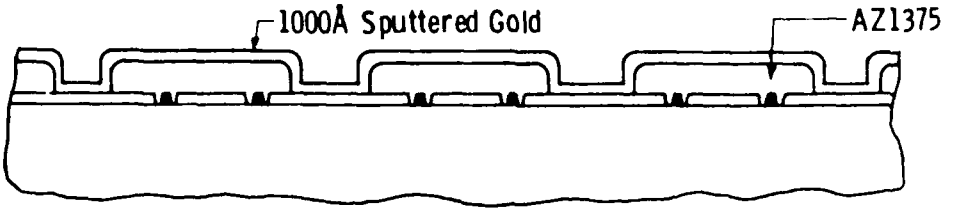


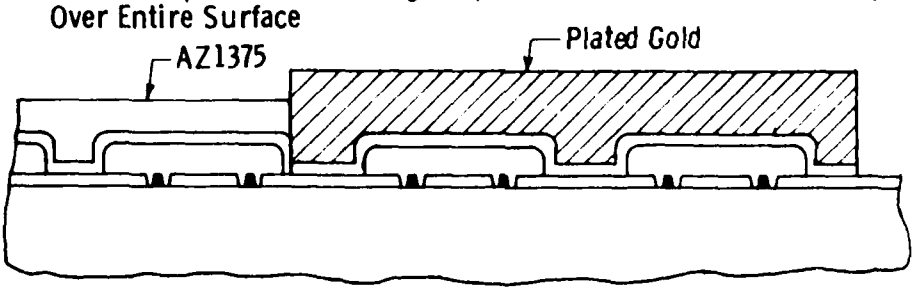
Figure 2-1. Steps in Via Fabrication



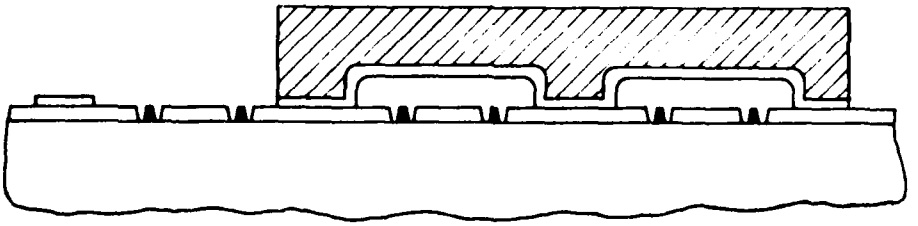
a) Wafer With Circuit Metallization Completed



b) AZ1375J Spacer for Air Bridge Deposited, 500 Å Ti + 500 Å Au Evaporated Over Entire Surface



c) Second Pattern of AZ1375, Gold Plated to 5 Microns



d) Photoresist Stripped, Air Bridge Formed

Figure 2-2. Steps in Air Bridge Technology

The resist is then exposed and developed to produce the airbridge pattern (see figure 2-2b). At this point, if the post-bake on the first layer is insufficient, there may be some wrinkling of the titanium-gold layer in those regions remote from the air bridge itself, but this is not critical.

Gold is plated onto the exposed titanium-gold portions at a current density of 3 mA/cm^2 for up to 3 hrs and a thickness of up to 6 μm using Selrex 401[2] commercial plating solution. The resulting structure is shown in figure 2-2c.

The top photoresist layer is removed by spraying with acetone, being careful not to attack the lower photoresist layer at this stage. The thin gold is etched for 30s in Metex Aurostrip at 55-60°C and the titanium removed in 15s in buffered HF at room temperature. The sample is then placed upside-down in boiling acetone for 15 min, which removes the lower photoresist layer. Any remaining residue, including photoresist under the bridges, is removed in an oxygen plasma to form the air bridges shown in figure 2-2d.

An air bridge fabricated in this manner is shown in a scanning electron micrograph in figure 2-3. The height of the bridge is 5 μm, its thickness is 6 μm, and its length 100 μm. The top picture shows a view looking under the air bridge, clearly demonstrating that the photoresist has been completely removed. The yield of these air bridges exceeds 95 percent. Air bridges formed between the sources of the imput transistor of a two-stage amplifier is shown in figure 2-4. Note also the inductors which form part of the matching circuitry are plated up at the same time as the air bridges.

Small-signal microwave measurements have been made on two 1200- μm periphery GaAs field-effect transistors that are identical in all respects except that one has air bridges and the other has wire bonds. The s-parameters are very similar, as shown in the Smith chart of figure 2-5. The term "sparse via" in figure 2-5 indicates that two vias were used to ground the outer most source pads of the devices and the remaining three pads of the 1200 μm FETs were grounded to these vias using air bridges or wire bonds.

The s-parameters were used in conjunction with an equivalent circuit model and the COMPACT [2] computer program to produce the element values shown in figure 2-6. From the model, it can be seen that the difference between the source inductance of the wire-bonded device (0.0344 nanohenries) and the air-bridged device (0.0337 nanohenries) amounts to 2 percent which is less than

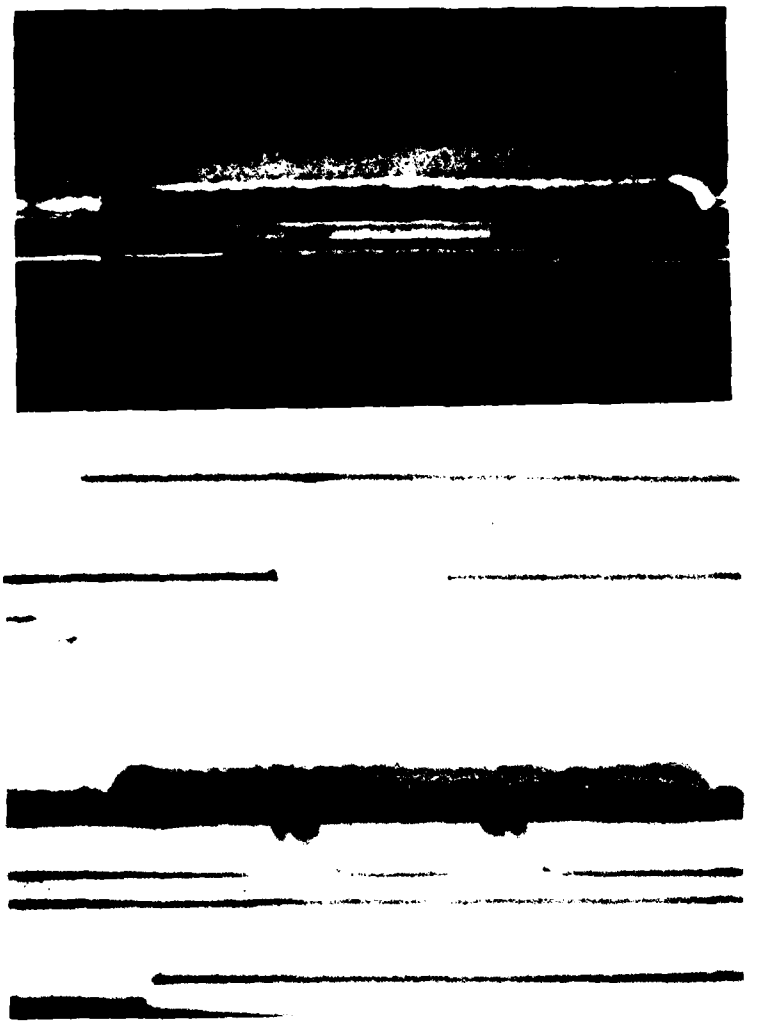


Figure 2-3. Six Air Bridge Interconnection on GaAs
Monolithic Circuit 5 um High, 6 um Thick, 100 um Long

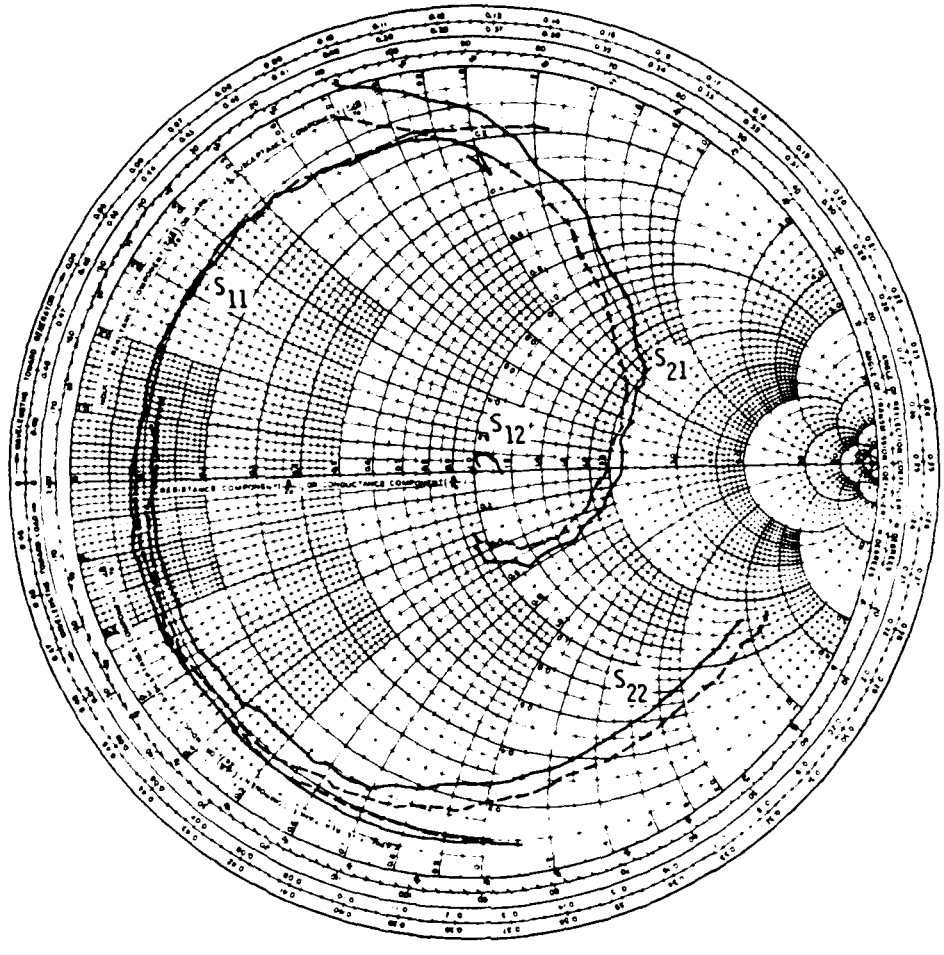


Figure 2-5. Comparative Microwave Characterization of 1200- μm FETs From Wafer IC26E: Wire Bond and Air Bridge Source Interconnections With "Sparse Vias"

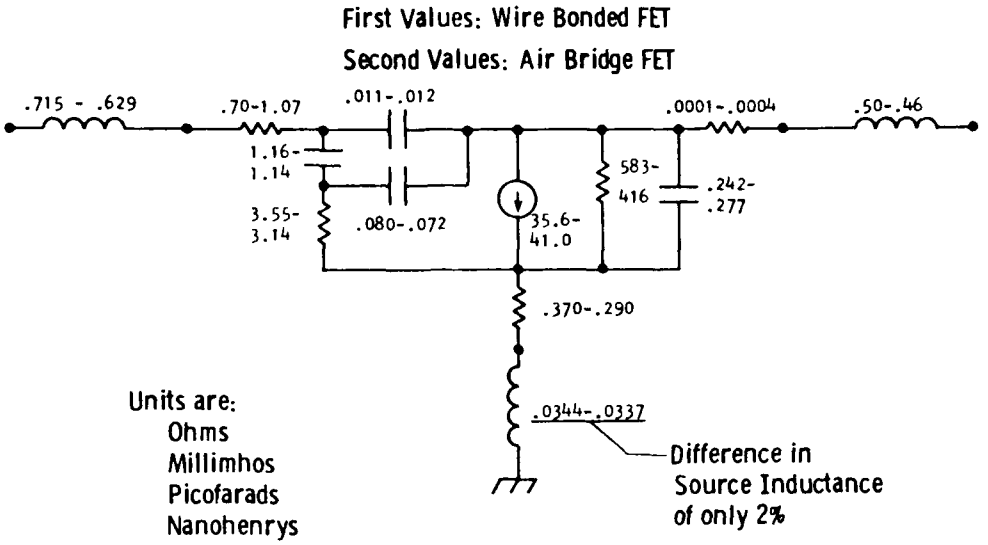


Figure 2-6. Comparison of Equivalent Circuit Valves of 1200- μm Periphery GaAs Power FET With Wire Bonds Versus One With Air Bridges

the variation of the other elements in the model. This indicates that the implementation of air bridges has in no way diminished the performance of the FET.

Air bridges will also be used in the fabrication of overlay capacitors as described in the following section.

2.2.3 Overlay Capacitor Technology

In the design and fabrication of GaAs microwave monolithic integrated circuits (MMICs), the metal-insulator-metal (MIM) overlay capacitor is a desirable component for dc bias line bypass and tuning circuit applications because it requires a much smaller area for a given capacitance than the interdigital capacitor and thereby allows larger capacitance values (2 pf → 20 pF) to be implemented on the chip. Design considerations for an overlay capacitor include the plate geometry, the properties of metals and dielectric films, and overall compatibility of fabrication with the existing GaAs IC technology.

a. Choices of Geometry, Metals and Dielectrics

The Q-factor of an overlay capacitor is dominated by the metal skin loss and the dielectric loss. For a typical overlay capacitor configuration, as shown in figure 2-7, Q for the skin loss in the electrodes is represented by Q_c as,

$$Q_c = \frac{3}{2\omega R_s (C/A)\ell^2} = \frac{3(W/\ell)}{2\omega R_s C} \quad (1)$$

where ω is the operating angular frequency; C is the capacitance; and R_s, A, ℓ, and W are sheet resistivity, area, length and width of the electrode, respectively.

b. Device Geometry

For gold electrodes with a thickness larger than the skin depth (~.8 μm at 10 GHz), the sheet resistivity (R_s) is 0.02 $\Omega/\square$ and Q_c for a 1 pF capacitor with a square geometry (W = ℓ) is higher than 1000, according to Eq. (1). For a 10 pF capacitor and a square geometry (W = ℓ), Q_c should be higher than 100 at 10 GHz.

c. Electrode Metals

Two important considerations for the electrode metals are compatibility with IC processes and the ability to maintain their physical integrity and electric conductivity during dielectric deposition. Ti/Pt/Au is used as the gate metallization of the GaAs power FETs and Cr/Pd/Au is the microwave circuit metallization. They are thus natural candidates for the bottom electrodes. Experiments have shown that Ti/Pt/Au maintains its physical integrity and high conductivity after being heated up to 450°C for 30 minutes on GaAs (figure 2-8), while Cr/Pd/Au degrades after such a high temperature treatment. Therefore, for low temperature deposition of dielectric films (e.g., sputtered SiO_2, sputtered Si_3N_4), both metallization systems are adequate as bottom electrodes. For dielectric films requiring high temperature deposition or curing (e.g., polyimide, plasma Si_3N_4), only Ti/Pt/Au is suitable. For top electrodes, either the overlay metallization or plated Au is suitable.

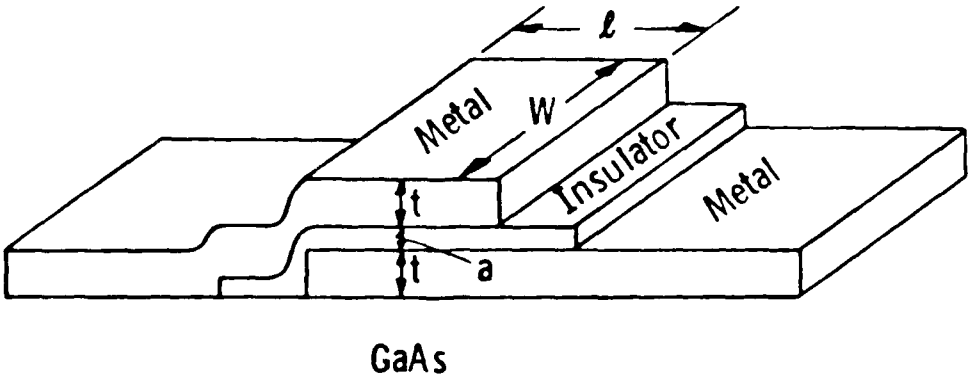


Figure 2-7. Configuration of a Metal-Insulator-Metal Capacitor

d. Dielectrics

Spun polyimide, plasma Si_3N_4, and sputtered SiO_2 have been used as dielectrics in the overlay capacitors. DuPont PI-2555 polyimide was applied to the wafer surface with a .2 μm-filtered syringe and spun to the desired thickness at a predetermined speed. After a partial cure at 120°C, the film was patterned with photoresist and etched in an oxygen plasma. Final curing was done at 300°C. Polyimide is very easy to apply - the application needs only standard photoresist equipment, and the film uniformity and reproducibility are excellent, but it suffers from a pinhole problem and is attacked by some chemicals used in the IC process (e.g., oxygen plasma and Metex gold etch). In addition, its C/A is lower than those of Si_3N_4 and SiO_2. For this reason, it has not been chosen for the IC process.

An LFE plasma-enhanced deposition system was used to deposit Si_3N_4 on GaAs substrates heated to 340°C. The film was subsequently patterned with photoresist and etched in plasma etcher using CF_4 gas. Si_3N_4 has a high dielectric constant (K = 7-8), low pinhole density, and is highly resistive to

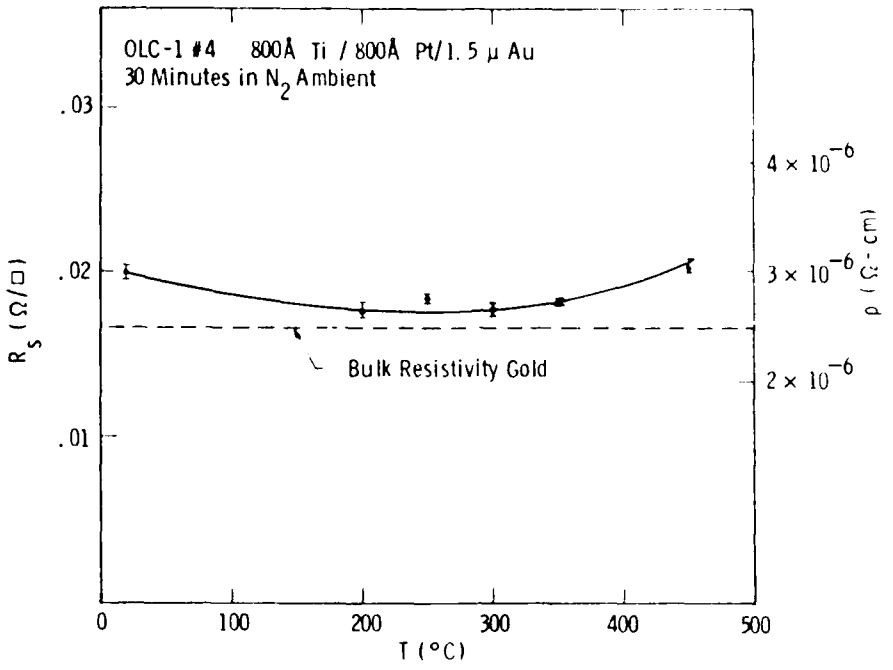


Figure 2-8. Resistivity vs. Annealing Temperature for a Ti/Pt/Au Metallization on GaAs

most chemicals, but it suffers from uniformity and reproducibility problems and a higher temperature deposition.

An MRC magnetron sputtering system with a rotating substrate plate was used to deposit the SiO_2 film. The dielectric constant of SiO_2 is acceptable (K = 4-5) and it has excellent film uniformity and reproducibility combined with very low pinhole density. This makes it the choice for our overlay capacitors.

e. Fabrication Procedure

The fabrication of sputtered SiO_2 overlay capacitors is compatible with and has been incorporated in the IC fabrication process. The bottom electrodes use a Cr/Pd/Au/Cr circuit metallization (the extra Cr metal on top is needed to improve adhesion of the dielectric film). The dielectric pattern is defined by AZ1350J photoresist with chlorobenzene-generated overhangs to facilitate the lift-off of sputtered SiO_2. 2500Å thick SiO_2 is deposited in the magnetron sputtering system, with a rotating substrate plate and compensating aperture for maximal film uniformity. During the deposition, a 50V bias is applied to remove loosely-held material from the substrate and the

SiO_2 film; this densifies the film and reduces pinholes. The reason for using lift-off to pattern the SiO_2 is to avoid sputtering damage to the FET channels and any attack of the ohmic regions by HF-based SiO_2 etches which would occur if regular etch-patterning techniques were used. The top electrodes for the capacitors are formed from plated gold at the same time that the air bridges are formed (see paragraph 2.1.2) and the top electrode is connected to the RF circuitry by an air bridge as shown in figure 2-9. The air bridge is used to avoid the problem of the upper contact metallization crossing the edge of the lower metallization. At this point, the dielectric is often thinner and premature breakdown may result in a shorted capacitor. An

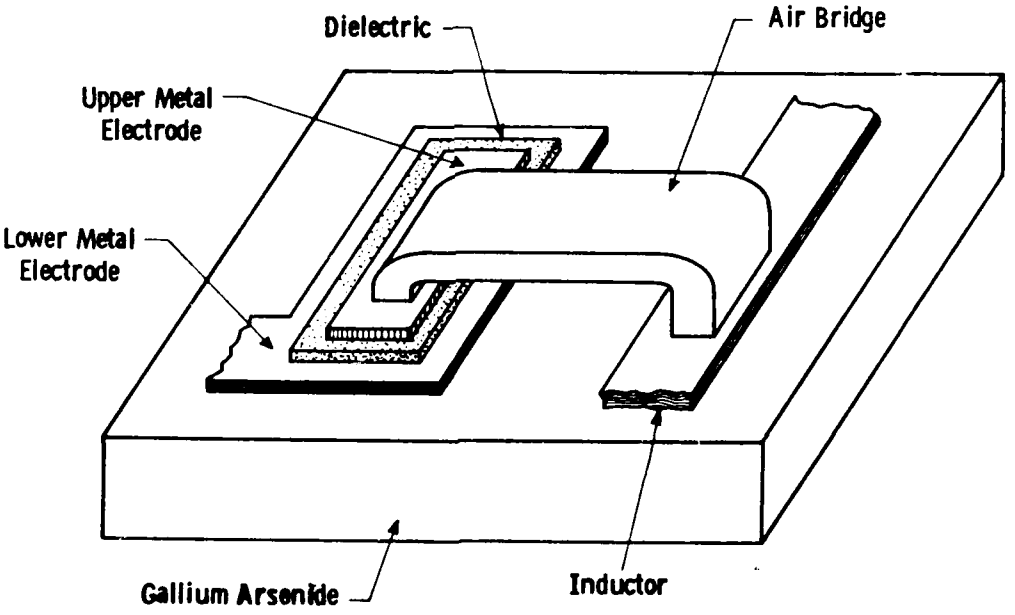


Figure 2-9. Overlay Capacitor With Air Bridge

SEM picture of a finished overlay capacitor is shown in figure 2-10.

f. Results of Measurements

Dielectric film thicknesses were measured with a Talystep™ profiling machine. Capacitances, breakdown voltages, and yields were measured at low frequency using probes with conventional C-V meters and curve tracers. Q-factors at microwave frequencies were measured by the reflection-resonance technique. The results on all three dielectrics are summarized in table 2-1. The combination of uniformity across a wafer, the 2 percent reproducibility of C/A, and a yield above 95 percent makes sputtered SiO_2 the choice over plasma Si_3N_4 or spun polymide, although all three capacitors show similarly high Qs at 8GHz.

Figure 2-10. SEM Picture of a Finished Overlay Capacitor

Table 2-1. Measurement Results of Overlay Capacitors Using Different Dielectrics

Dielectric	Sputtered SiO_2	Plasma Si_3N_4	Spun Polyimide
Thickness	2500Å	2500Å	4000Å
Dielectric Constant (K)	4.24	7.06	3.70
C/A (pF/mm^2) over a 2" wafer	150 ± 4.5 (3%)	250 ± 25 (10%)	82 ± 1.5 (2%)
Reproducibility from wafer to wafer	2%	6%	1%
Yield for 5 pF Capacitors	>95%	>95%	75%
Breakdown Voltage	>100 volts	>100 volts	>100 volts
Q at GHz	30.5	28.5	32.4

2.2.4 Monolithic Resistor Technology

The design of the 3 watt output stage that will be described in paragraph 3.2 requires the implementation of resistors to provide isolation between the various 800- μm device cells. The choice of resistor technology lies between thin metal resistors, such as nichrome or titanium, deposited on the semi-insulting gallium arsenide in a separate fabrication step or an ion-implanted active gallium arsenide area with ohmic contacts. The latter type has been chosen using the same implant profile as that employed for the FETs in the amplifier structure. The advantage of this approach lies in the fact that it introduces no additional steps in the fabrication procedure.

Since the resistor must be linear over the voltage range of interest ($\sim$ 10 volts), the current in the resistor structure must not saturate in this voltage range. For a 10-volt maximum operating point, the ohmic contacts for the resistor must be spaced by at least 36 μm so that the saturation field of 2.8 kV/cm is not exceeded.

The sheet resistance of the layers implanted for the GaAs power FETs is typically 450 Ω/square so that for a resistance of 50 Ω, an aspect ratio of 9:1 is required. This, combined with the 36- μm spacing between ohmic contacts, produces a resistor with the dimensions of 36 x 324 μm. While this

resistor is large when compared with some other components of the circuit, its ease of implementation justifies its use. Test resistors have been fabricated using ion implantation and figure 2-11 shows the current-voltage characteristics of a 500 Ω resistor with a dynamic range of 10 volts.

2.2.5 Wafer Thinning

After the circuit metallization is completed, the wafer is thinned from its starting thickness of 625 μm to 100 μm. The value of 100 μm was chosen so that the width of the circuit elements on the monolithic circuit may be kept to reasonable values to achieve the desired impedance without excessive losses, while the thermal impedance of the transistors in the circuit is sufficiently low (8.6°C/W/cm) with this thickness of GaAs to keep the temperature rise to less than 108°C. The final criterion for the thickness of the gallium arsenide substrate is that via connections must be etched through the substrate to ground certain areas of the circuit directly to the substrate.

The thinning of the wafer has been accomplished using the semiautomatic jig shown in figure 2-12. A wafer support disk consisting of a silicon wafer or a sapphire plate is first mounted to the base of the lapping jig using AZ1350 photoresist which is baked at 90°C for 60 min. The gallium arsenide wafer is then mounted onto the support disk using wax which melts at 60°C. The lapping disk is then screwed into the bottom of the plunger at the center of the lapping jig as shown in cross section in figure 2-13. The plunger is inserted into its housing and the whole mechanism is placed on a reciprocating glass table covered with a slurry of 3 μm grit in water and lapped until the thickness reaches within 12.5 μm above the required final thickness. The amount of material removed is monitored using the micrometer gauge attached to the plunger. A polish down to the final thickness is then performed on a rotating polishing pad using 0.5 percent bromine in methanol. The gallium arsenide wafer plus carrier can now be removed from the lapping disk by dissolving the photoresist in acetone. The lapping procedure results in excellent thickness uniformity. This is indicated in figure 2-14 which shows two partial wafers with 2-in. dimensions that have been polished down to 75 μm thickness with a uniformity of 2.4 and 5 percent.

2.3 SUBMICRON POWER FET DESIGN

The X-band power FET design is based on a 0.7 μm gate length cell with a 100 μm unit gate width. The program goal is a 3-watt amplifier operating from

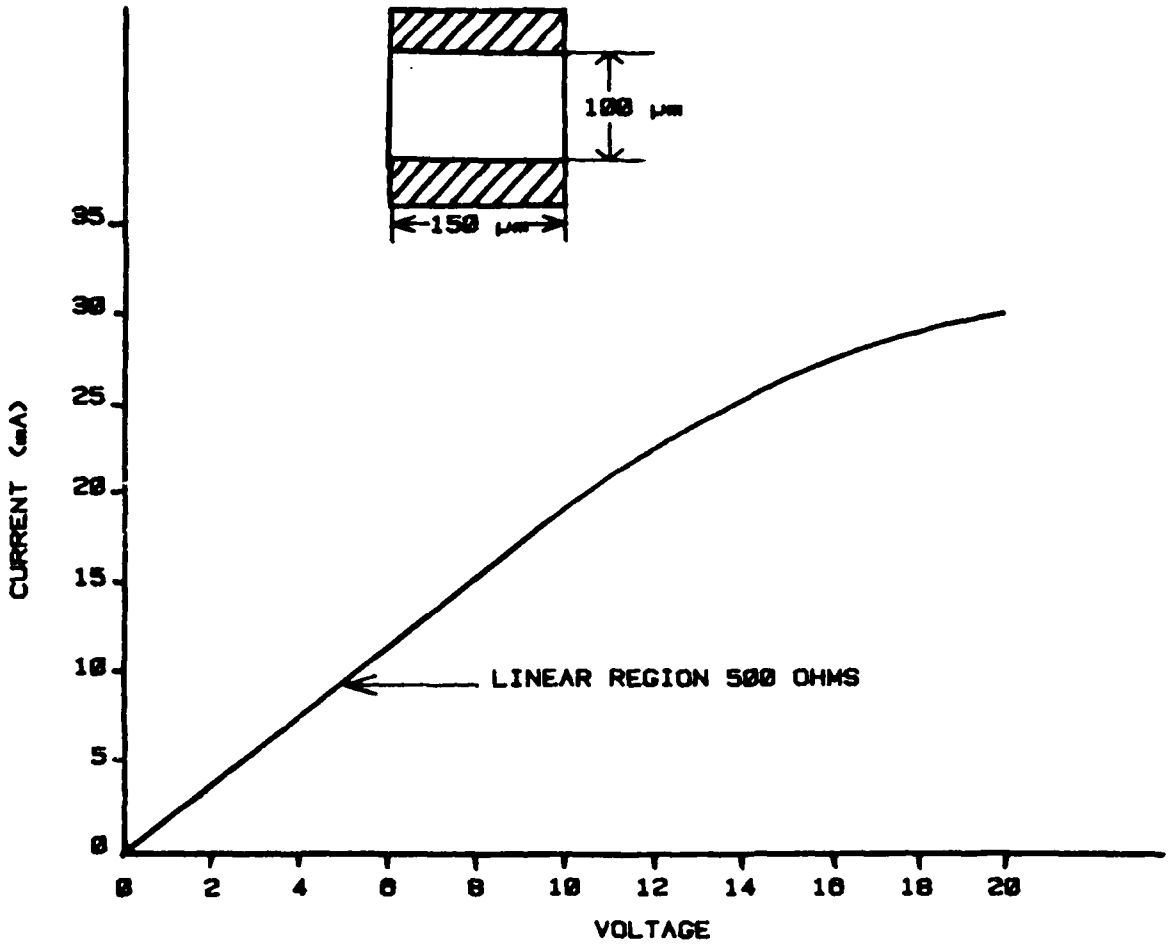


Figure 2-11. Current-Voltage Characteristics of a 500Ω Implanted Resistor

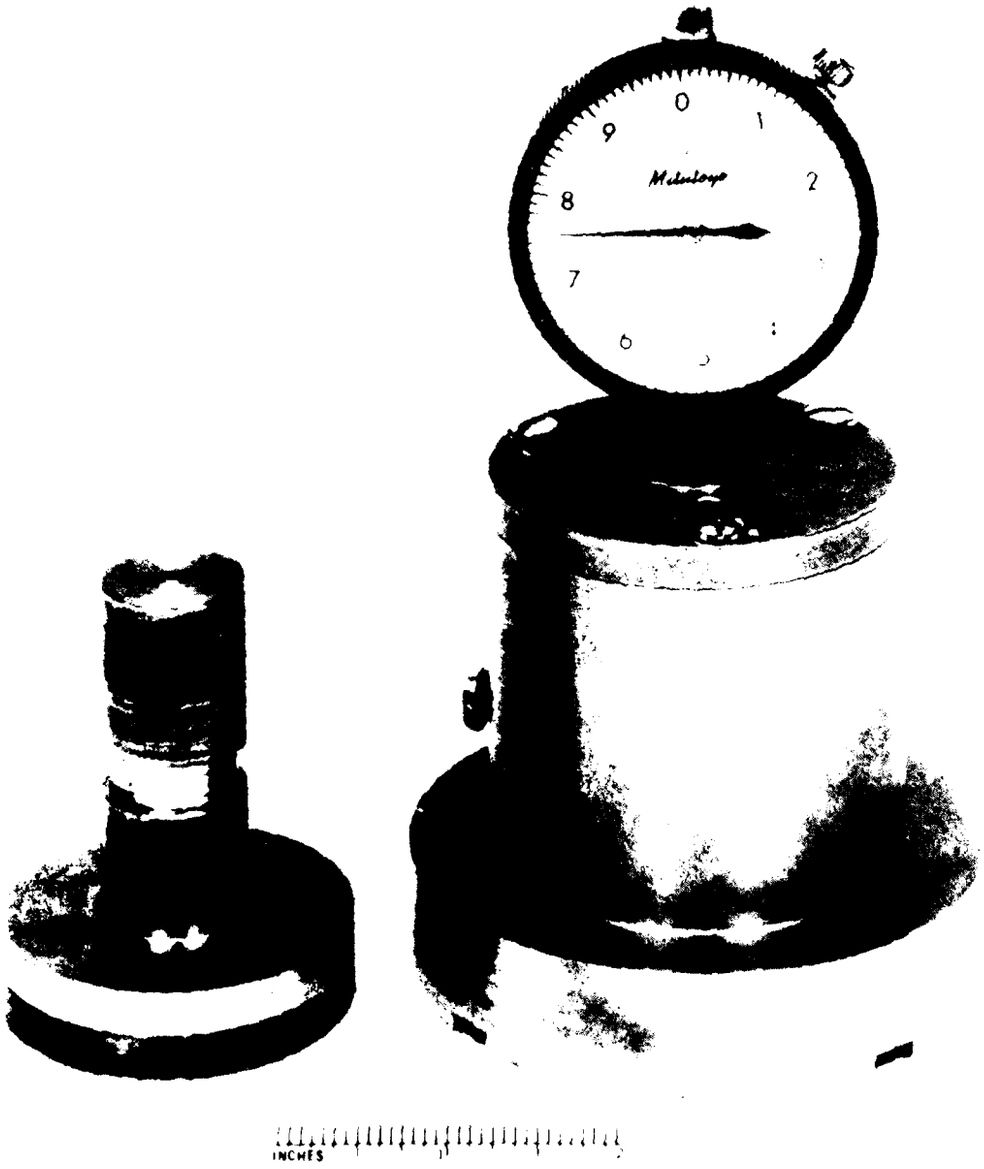


Figure 2-12. Semiautomatic Lapping Jig

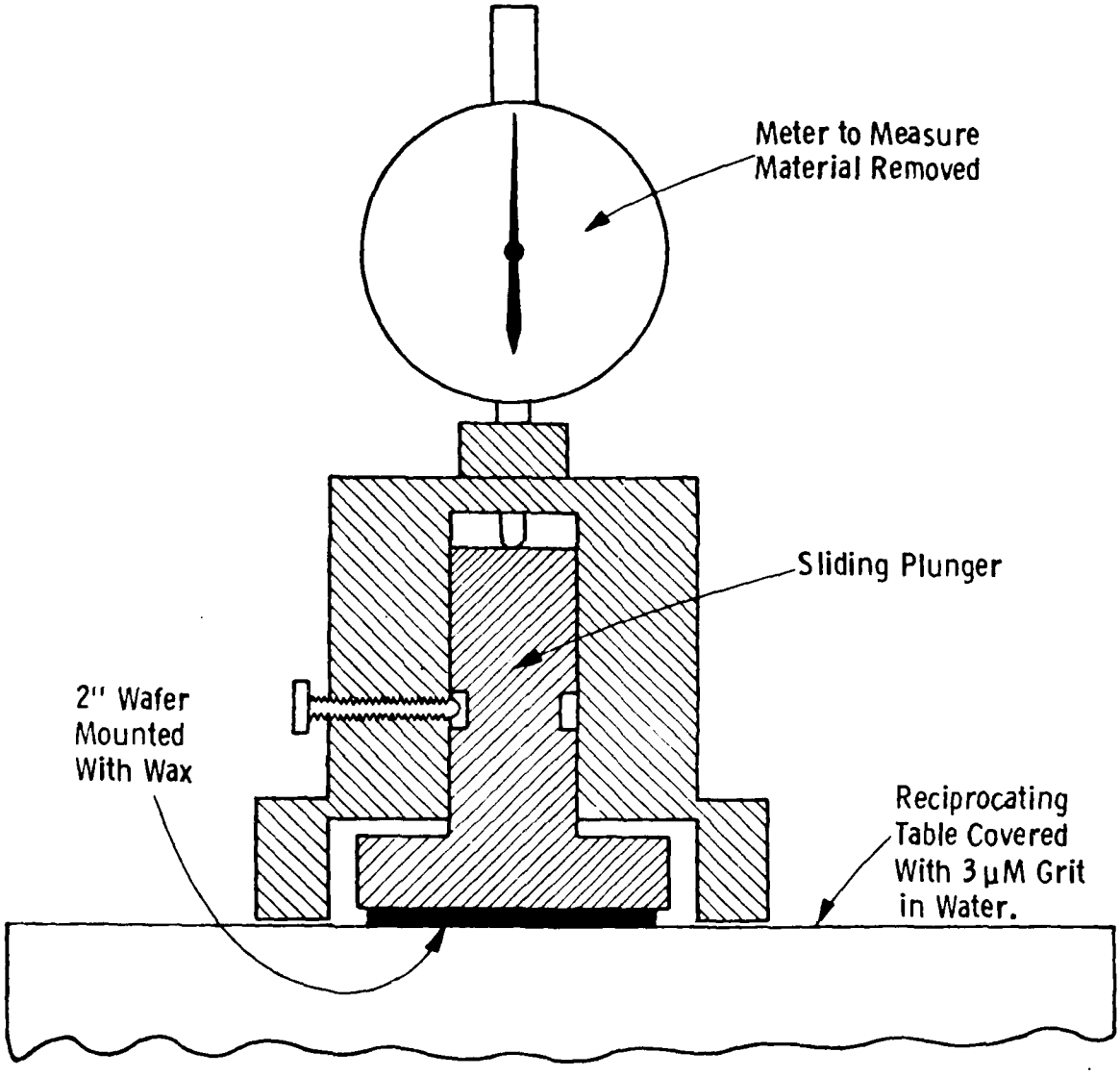


Figure 2-13. Cross Section of the Lapping Jig

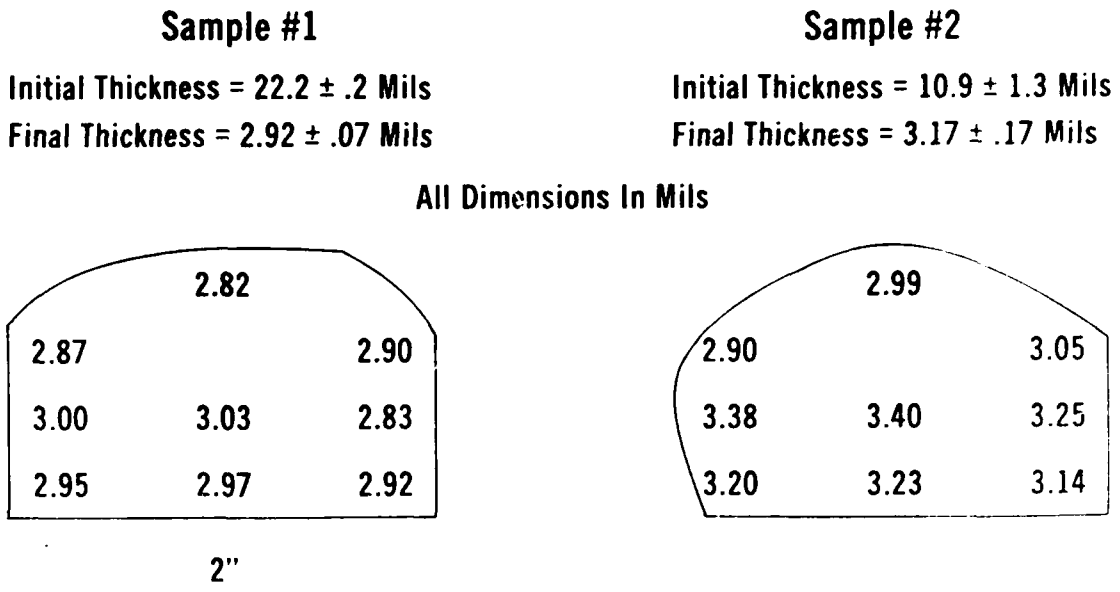


Figure 2-14. Uniformity of GaAs Wafers After Lapping and Polishing

8 to 12 GHz with 20 dB associated gain. The power gain performance of the previous FET cell with 1- μm gate and 150- μm width was inadequate to meet the program goals at 12 GHz; hence, a new design was required. One approach to improving device gain is to shorten the gate length in order to reduce the gate-source capacitance. The introduction of deep UV lithographic technology (described in paragraph 2.4) has allowed the design of devices based on 0.7 μm rules. However, in order to determine the implications of thermal effects, unit gate width, and gate geometry on power gain performance, a number of discrete power FETs were designed. In addition to our standard test cell (FAT FET, contact resistance, gate resistance, Hall cloverleaf), 24 different FET geometries were included in the master field. This includes a variety of device peripheries (300 to 2400 μm), unit gate widths (75 to 150 μm), and source-drain contact geometries.

2.3.1 Device Geometrical Considerations

Figure 2-15 shows a 1200- μm power FET successfully used in the monolithic 5 - 10 GHz power GaAs amplifiers. The device has 1-mil wide drain

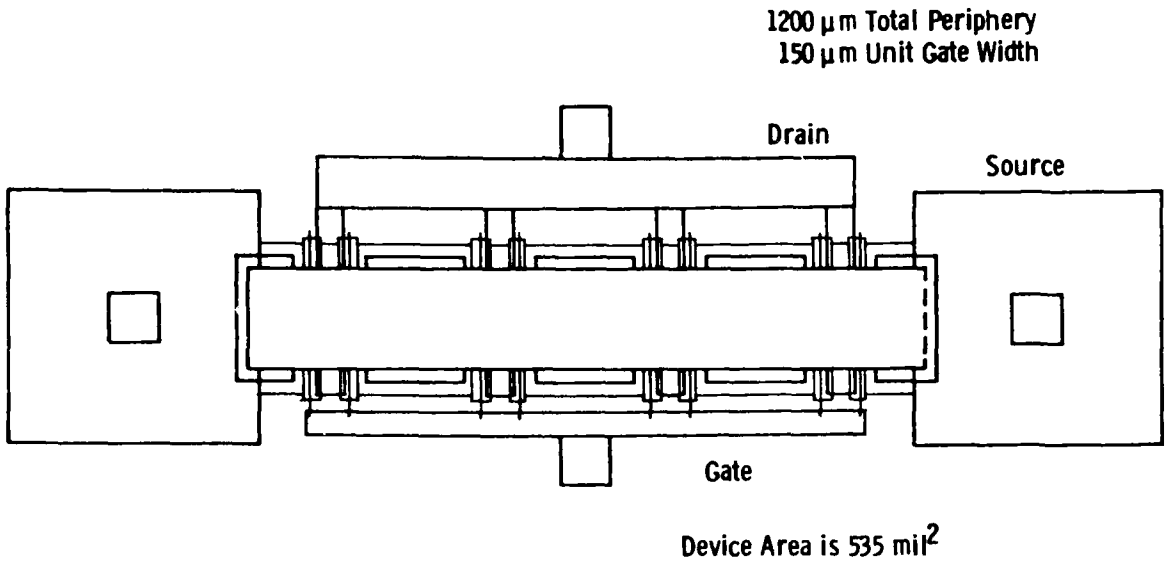


Figure 2-15. Assymetrical Source and Drain Pad Power FET

pads, 5-mil wide source pads, 150- µm gate width, and a 1- µm gate length on eight parallel fingers. Because the gate finger acts as a distributed transmission line, there is a relative phase shift in the RF voltage along each gate finger. In order to determine the advantages of shorter unit gate widths, devices with 75 and 100 µm unit gate widths were included in the mask set.

Shortening the unit gate width requires an increase in the number of cells for a constant periphery FET. This greater number of cells will occupy too large an area unless one also minimizes the source and drain pad size. The device shown on figure 2-15 was designed with 5-mil source pads to allow via connection of each source pad to ground. This RF grounding scheme (total via grounding) minimizes the parasitic source inductance to ground, which in turn maximizes the power gain. But, grounding every source pad is costly in device area and requires very high yield of via holes. On the basis of previous work, via grounding of the end source pads was combined with air bridge interconnects to provide a reproducible, high yield source interconnection technology ("sparse via FET").

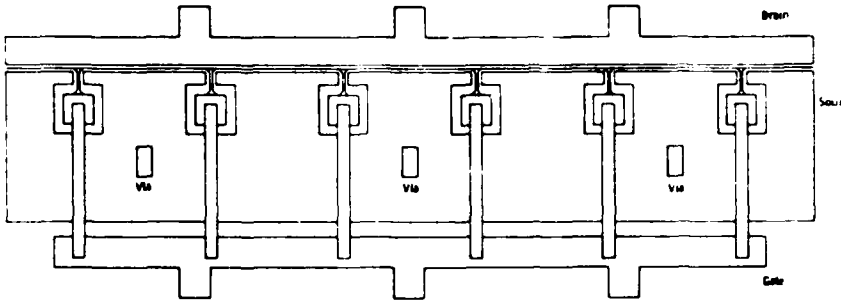
In order to minimize the source and drain pad area without degrading the device thermal impedance, it was necessary to carefully calculate the thermal impedance of new geometries. The device shown in figure 2-15 was designed with a small drain pad and a large source pad for via grounding of each source. This assymetrical pad scheme leads to a 47°C/W-mm thermal impedance for a 150- μm unit gate width on 4-mil thick GaAs. For a device constructed with identical source and drain pads, it is possible to employ 2-mil wide pads to obtain a similar thermal performance. Thus, devices were designed with 2-mil source and drain pads to minimize the air bridge inductance, maintain the previous thermal performance, and reduce the total source and drain pad width from 150 μm to 100 μm.

An alternative geometry FET was suggested as a means to prevent mutual coupling between parallel gate fingers. This type of device (Pi Gate FET) is shown in figure 2-16a. Figure 2-16b shows an equal periphery parallel feed device for comparison. It is important to note that the Pi Gate device should yield gain performance equivalent to the total via parallel gate feed device, while occupying an area 35 percent larger than the sparse via device shown in figure 2-16b. Thus, the Pi gate device provides a potential power gain improvement over the sparse via parallel gate feed device because of improved via grounding and minimal gate-gate coupling effects. The device thermal impedance is independent of unit gate width and is estimated to be 45°C/W-mm. This figure was obtained by treating the Pi gate FET as a parallel gate feed device with infintely long unit gate width, infinite gate-to-gate spacing, and a 4-mil thick GaAs substrate.

2.3.2 Discrete Power FET

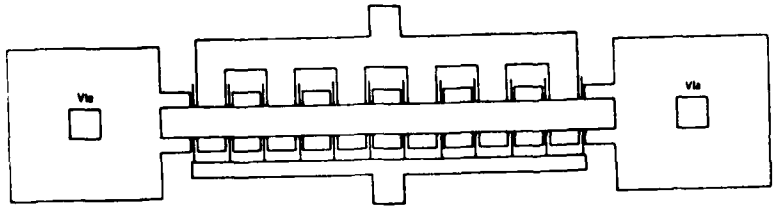
a. Mask Layout

As mentioned in paragraph 2.3, the master field of the discrete power FET mask contains 24 different FET geometries. All the devices were designed with nominal 6.5 μm source-drain spacing and 0.75 μm gate length. The gates were offset 1 μm closer to the source than the drain. Table 2-2 gives the distribution of device peripheries for sparse via and pi gate power FETs with the device unit gate width as a parameter. The five footnotes in table 2-2 detail the apparent redundancy for a certain periphery and unit gate width combinations. A resistive feedback device was included as an RF test vehicle for implanted resistors. The majority of sparse via devices were



1200 µm TOTAL PERIPHERY
100 µm UNIT GATE WIDTH

A Pi-Gate FET - Device Area is 733 mil^2



1200 µm TOTAL PERIPHERY
100 µm UNIT GATE WIDTH

B Sparse Via FET - Device Area is 537 mil^2

Figure 2-16. Comparison of Pi Gate and Sparse Via Power FET Geometries

Table 2-2. Discrete Power FET Geometries Included in Master Field

Total Periphery µm (Unit Gate Width as a Parameter)	"Sparse Via" Parallel Gate Feed Power FET	"Pi Gate" Power FET
300 µm	2 @ 75 µm	3 @ 75 µm
400 µm	2 @ 100 µm	
600 µm	2 @ 75 µm 1 @ 75 µm[1] 1 @ 100 µm 1 @ 100 µm[2]	2 @ 100 µm
1200 µm	1 @ 75 µm 1 @ 100 µm 2 @ 150 µm 1 @ 150 µm[3]	1 @ 75 µm 1 @ 75 µm[4] 2 @ 100 µm 1 @ 150 µm 1 @ 150 µm[5]
1500 µm	1 @ 75 µm 1 @ 150 µm	1 @ 150 µm
1600 µm	1 @ 100 µm	1 @ 100 µm
2400 µm	1 @ 100 µm	1 @ 100 µm

1 - Resistive gate-drain feedback device.
2 - Cascode FET combination.
3 - Assymetrical source and drain (Figure 2-15)
4 - Air bridge source interconnection (Figure 2-17a)
5 - Gate bus interconnection without air bridge (Figure 2-17b)

designed using 2 mil source and drain pad design rules as detailed in paragraph 2.2.1. For thermal comparison, one device was included with the older assymetrical pad geometry shown in figure 2-15. The Pi Gate FETs have individual geometrical variations owing to unit gate width choice. Figure 2-17 gives an example of two Pi gate FETs which are unique compared to the device shown in figure 2-16a. The FET of figure 2-16a has 100 μm unit gate width, total via source grounding, and air bridge gate bus interconnection. The FETs in figure 2-17 have 75 and 150 μm unit gate widths, respectively. The 75- μm unit gate width device requires a combination of air bridges and vias for source grounding. Conversely, the 150- μm unit gate width Pi gate FET has adequate area to permit total via grounding while eliminating the requirement for air bridging of the gate bus interconnection.

The master field is 0.330 x 0.305 in. and is stepped and repeated approximately 33 times for a 2-in. round substrate. The geometries included have provided us with data to make the following conclusions:

1. Via technology yield exceeds 99 percent for the various pi-gate and sparse-via geometries investigated.

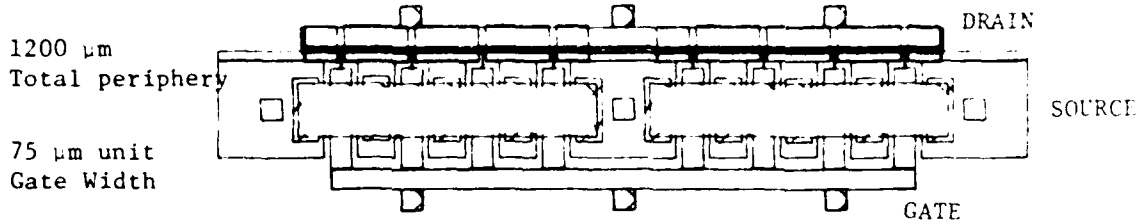
2. Thermal impedance evaluation for the change from assymetrical to symmetrical pad geometry FETs requires detailed measurement; however, device power performance is indistinguishable between the two geometries.

3. Measurements of device performance through 12 GHz has failed to show an advantage between 75 and 100- μm unit gate width devices.

4. No distinction has yet been observed between Pi-Gate and sparse via FETs up to 12 GHz. It is believed that further comparison of RF results or operation at higher frequencies is necessary to determine any relative advantage between these two device geometries.

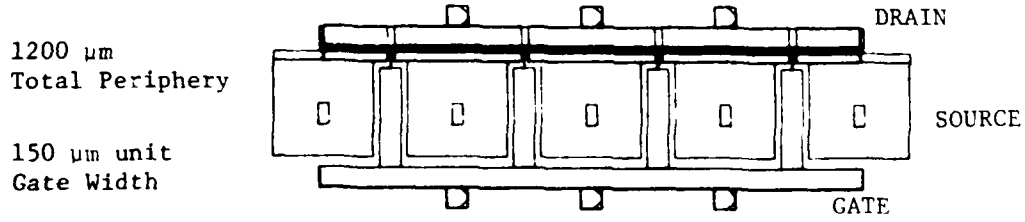
2.3.3 Device Design for 3-Watt, 8-12 GHz Amplifier

To provide 3 watts of RF power from the final stage of the required monolithic amplifier (8-12 GHz, 20 dB gain, 3 watts), it is necessary to optimize the choice of cell configuration and power FET periphery. Assuming a 0.5-dB loss in the output matching circuitry, the output FET must deliver 3.37 watts. Allowing for less than perfect tuning in the broadband power matching, it was decided that a 0.6 watt/mm FET performance requirement at12 GHz was a goal consistent with laboratory experience. Thus, a 6400- μm power FET is necessary for the 3-watt amplifier. As discussed in section 3, a



Device Area is 1155 mil^2

A "Pi Gate" FET with Air Bridge and Via Source Interconnection



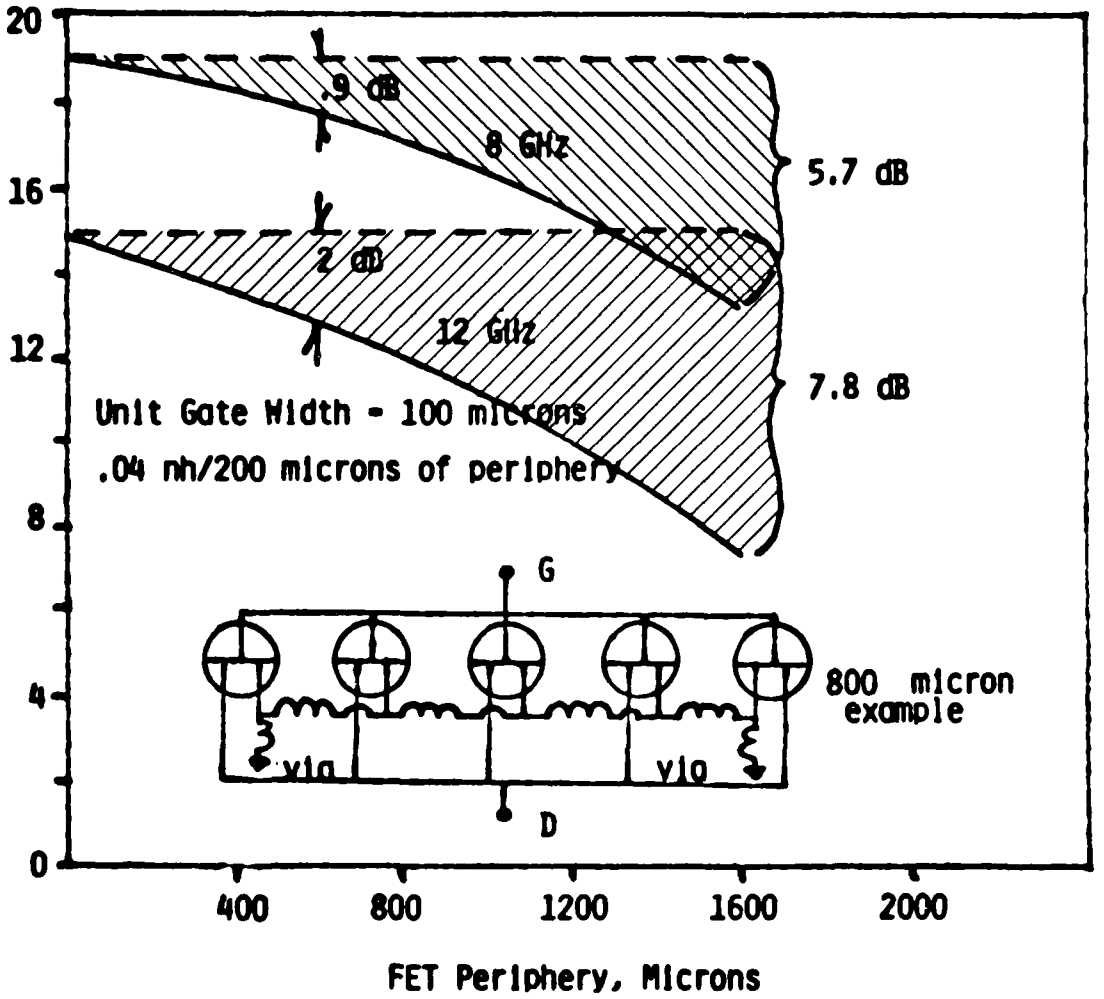
Device Area is 900 mil^2

Figure 2-17. Comparison of Two Pi-Gate FETs With Identical Total Periphery and Different Unit Gate Width

6400- μm FET can be properly loaded only by matching internal clusters followed by broadband combining sections. The choice of device unit gate width between vias was determined by observed 12-GHz gain performance and the necessity to minimize total FET area. Data shows that the 75- μm and 100- μm gate width FETs outperform the 150- μm unit gate width devices at 12 GHz. As discussed in paragraph 2.3.2, no significant gain advantage has been observed at 12 GHz between the 75 μm and 100 μm cells. Therefore, consistent with the desire to minimize FET area, the 6400- μm device was designed using 100- μm unit gate width cells.

In order to determine the optimum cluster periphery, a computer modeling of FET cell combination was done using COMPACT. As discussed in paragraph 2.3.1, the choice of source grounding techniques and physical geometry are sources of possible gain degradation. By employing COMPACT, the gain degradation associated with via and air bridge placement was studied. Figure 2-18 shows the results for 100 μm unit gate width, parallel gate feed FETs. For a total via device, MSG is independent of periphery (neglecting any phase change between cells) and is 19 dB at 8 GHz and 15 dB at 12 GHz. For a device with end vias and air bridge interconnects, gain degradation becomes a dramatic function of periphery due to air bridge inductance connecting the cells. Referring to figure 2-18, a 1200- μm sparse via FET suffers a 6.2-dB gain degradation at 12 GHz compared to the total via FET. By reducing the cluster size of sparse via devices to 800 μm, the model predicts only 3-dB gain loss compared to a total via FET. The 800- μm device is a good compromise between gain degradation and the total number of individual clusters.

The Pi Gate FET has not yet shown any gain or power advantage over the sparse via geometry. In order to provide further data regarding the relative merits of the two geometries, the 3-watt amplifier has been designed using both device types. The 3-watt IC mask includes a center dropout containing 18, 800- μm Pi gate FETs and 18, 800- μm sparse via FETs for test purposes. The data from these discrete devices will be correlated with the 3-watt amplifier performance to determine if the Pi gate device has any advantage over the sparse via FET.



– – – "Total Via" FET Source Ground

——— "Sparse Via" FET Source Ground

Figure 2-18. Gain Degradation of GaAs Power FETs as a Function of Device Periphery Due to Source Inductance at 8GHz and 12GHz

2.3.4 Implant Profile

The range of frequencies for the four-stage amplifier in this program is from 8 to 12 GHz, which requires a gate length for the FETs of 0.7 μm. The previous program (N00014-78-C-0268) specified a lower frequency range (5 to 10 GHz) and the FETs used a correspondingly longer gate (1 μm). In table 2-3 are shown a comparison of the various implant parameters for the two FET designs.

Table 2-3 Comparison of Implant Parameters for Two FET Designs

	1.0- μm FET	0.7- μm FET
Deep Implant Dose (x $10^{12}/cm^2$)	3.9	4.4
Deep Implant Energy (KeV)	275	250
Peak Concentration (cm^{-3})	1.3×10^{17}	1.5×10^{17}
Depth of 1/2 Peak Concentration (Å)	3200	2850
Shallow Implant Dose (x $10^{12}/cm^2$)	1.3	1.3
Shallow Implant Energy (KeV)	125	125

As can be seen from the table, the implant dose has been raised 13 percent while the energy has been lowered 9 percent. The result of this is to provide a shallower implanted layer profile with a higher peak carrier concentration both of which will improve the performance of the amplifier at the high (12 GHz) end of the frequency range. The shallow surface implant remains unchanged.

2.3.5 Discrete FET Measurements

Paragraphs 2.2.1 and 2.2.2 described the design and mask layout for discrete FETs which are intended to provide the data necessary for the design of the four-stage, 3-watt amplifiers and, in particular, the initial designs of the 3-watt output stage. In this section are described the results of three fabrication runs using the discrete mask set plus the results of measurements made on discrete devices fabricated at the same time as two runs of two-stage amplified (IC 31 and IC 32).

The initial runs (IC 31, IC 32, and D38) were all made using long wavelength (4050 Å) illumination to expose the gate openings in AZ 1350 J photoresist. IC 31 and IC 32 had 1 μm gate lengths, while runs [illegible] and D 38 used an E-Beam mask fabricated on a 0.090-in. quartz blank with 0.75-μm

(nominal) gate lines. This mask was later used with deep UV (2100 Å) exposure and PMMA to form submicron lines in run D 39.

A problem occurred during the evaporation of ohmic contacts to run D 36 when trapped gases in the platinum source used for the platinum evaporation caused spitting of that metal and the deposition of platinum balls up to 30 μm in diameter on the top surface of the gold-germarrium/nickel/platinum metallisation. With the balls present, intimate contact between the mask and the wafer was not possible resulting in gate lengths of 1.3 to 1.5 μm instead of the 1 μm that was desired. Fabrication was completed on these devices as a first test of the new mask set.

Run D 39 involved the use of the deep UV system for the first time on this program. A single layer of PMMA 1 μm thick was exposed using 2100Å radiation and developed to produce 0.7-μm opening. An example of a gate produced by lift-off of this PMMA is shown in figure 2-19.

Figure 2-19 Example of a 0.7 μm Long Gate From Run D 39 Formed Using a Single Layer of PMMA and Deep UV Exposure

2.3.5.1 DC Characteristics

Average values of the material and device characteristics of the five runs are shown in table 2-4. The majority of the implants were made at 275 KeV for the deep implant and 125 KeV for the shallow implant. This latter implant is intended to bring the surface concentration up to above 10^{17} cm^{-3} where contacts will have sufficiently low ($< 3 \times 10^{-6\Omega}$ cm^2) contact resistance. Run D 39 contains wafers implanted at 250 KeV, for the deep dose which reflects the need for a shallower, higher concentration profile for device operation at 12 GHz.

The saturated drain currents are measured after the ohmic contacts have been deposited and alloyed, but before the gate recess is etched and the gate metal deposited. For the five runs shown in table 2-4, the drain currents range from 415 to 622 mA/mm. The design valve for the current at this stage is 566 mA/mm for a carrier concentration of 1.2×10^{17} cm^{-3} and 651 mA/mm for $1.6 \times 10^{17}/cm^{-3}$. After gate recesses of 600Å to 800Å, these valves are expected to drop to 430 mA/mm and 466 mA/mm, respectively. Specific contact

Table 2-4. Material and Device DC Characteristics of Discrete Device Runs

RUN NO	IMPLANT DOSE $X10^{17}$ (CM^{-2})	IMPLANT ENERGY (KEV)	PEAK CONC. $X10^{17}$ (CM^{-3})	DEPTH AT ½ PEAK (Å)	DRAIN CURRENT (BEFORE GATE RECESS) (MA/MM)
IC31	4.2/1.4	275/125	1.1	3300	480
IC32	3.9/1.3	275/125	1.1	3150	500-533
D36	4.05/1.35	275/125	1.3	3300	667
D38	4.35/1.35	275/125	1.3	3300	433-600
D39	4.5/1.5	250/125	1.6	2850	622*
	4.5/1.5	275/125	1.1	3300	415

*HIGH SURFACE ACTIVATION DUE TO Si^{29} (125 KEV) CONTAMINATION

82-2381-TA-1

resistances have been measured using test patterns from the runs D 38 and D 39 giving the valves 3×10^{-6} and $\sim 2 \times 10^{-6\Omega}$ cm^2, respectively except for one wafer from D 39 where the peak carrier concentration is low (1.1×10^{17} cm^{-3}).

Two wafers from run D 39 had higher surface implants than desired due to the improper operation of the implanter. This yielded a high surface concentration and a profile that fell monotonically with distance in to the implanted wafer.

2.3.5.2 Small Signal Gain and Power Output

The results of small signal gain and power gain measurements made on the five runs are shown in table 2-5. The values represent the best results obtained on each run and the power output is measured at 4 dB of gain. On those devices with power outputs of less than 400 mW/mm (see runs IC 31, IC 32 and D 38), the power output was not measured up to 12 GHz. Run D 36 had the best power output, exceeding 600 mW/mm up to 10 GHz and in one small device (300 μm periphery) had almost 600 mW/mm at 12 GHz.

The gains of the devices in run D 36 were low (~ 2 dB) due in part to the longer gate lengths (1.3 to 1.5 μm) of this run.

Table 2-5. Small Signal and Power Measurements on Discrete Devices

RUN #	PERIPHERY (μM)	GAIN AT GHz			POWER OUT (MW/MM)		
		AT 8 GHz	10 GHz	12 GHz	8 GHz	10 GHz	12 GHz
IC31	1200	13.0	10.5	7.8	393		
IC32	1200	12.1	10.2	UNSTABLE	290	136	
D36	1200	9.93	UNSTABLE	UNSTABLE	615	558	146
	600	11.0	10.3	UNSTABLE	797	756	390
	300	13.2	9.0	UNSTABLE	660	633	593
D38	1200	12.7	9.15	UNSTABLE	241		
D39	400	18.0	UNSTABLE	UNSTABLE	393	429	421

82-2381-1A-2

Run D 39 is the first run fabricated using the deep UV process and shows power outputs approaching 400 mW/mm up to 12 GHz.

2.3.5.3 Discussion

The power per unit periphery at 12 GHz obtained from FETs in this series of discrete device fabrication runs is lower than the 500 mW/mm program goal. Runs IC 31, IC 32, D 38, and D 39 had lower drain currents than are required for optimum gate recess ($\sim 800\text{Å}$). The exception was one wafer from D 39 that had high surface activation due to an excessive low energy implant dose, but the resulting profile effectively had a long tail and therefore provided poor power performance.

Run D 36, which had good implant activation and sufficiently high drain currents, had a long gate length (1.3-1.5 μm) due to the platinum spitting problem and, hence, although the power output was good, the gain was too low to be useful at 12 GHz.

As the deep UV gate technology becomes further refined, the regular achievement of submicron gate length power GaAs FETs is expected to satisfy the program goals. The results of run D 39 with > 400 mW/mm up to 12 GHz is encouraging in this regard.

2.4 DEEP UV PHOTOLITHOGRAPHY

GaAs FET gates, 0.7 μm in length, have been fabricated by the lift-off technique. The advantages of lift-off include freedom from possible substrate damage during etching, great versatility, rapid design turnaround time, and low cost. The main disadvantage is that the photoresist mask, with its overlying metal, must be removed without damage to the gate patterns deposited directly on the GaAs substrate. This secondary operation is best performed by dissolving the underlying photoresist so that the unwanted metal is dislodged from the wafer. Positive type photoresists, unlike negative types which experience cross-linking during exposure, are easily dissolved in strong solvents such as strippers and the carrier solvents in the original photoresist formulation. Solvent polarity and molecular size are important parameters in selecting suitable solvents. AZ1350 is an excellent positive-type photoresist which dissolves very rapidly in acetone. Positive-type deep UV resists such as PMMA, PMIPK, P(MMA-MAA), and PCA all have solvent systems which readily dissolve them, even when they have not been exposed.

The solvent system must contact the resist directly in order for dissolution to occur; this is not always possible after metal deposition unless special precautions are used to keep the deposited metal away from the edges of the resist mask. These precautions include using resist films thicker than the deposited metal, collimating the metal deposition system, and controlling resist edge profiles. Resist profiles ideally have negative slopes; i.e., the resist has the appearance of being undercut. Negative slopes are theoretically possible in positive-type resist systems exposed by deep-UV contact printing because diffraction causes the light to diverge under the mask as it passes the chrome edge.

Simply reasoned, this effect would produce an undercut resist profile. Unfortunately, the intensity of the deep UV radiation is not constant since the total photon flux is limited by the mask aperture. The diffracted light inevitably brings on a smearing of the ideal exposure profile, as shown in figure 2-20. The diffraction patterns are predicted by the Fresnel-Kichhoff scalar theory of diffraction and Skinner* of BTL has plotted several profiles for one-dimensional slits based on a parameter Q defined by $Q = W\sqrt{2/\lambda g}$, where W is mask aperture (μm), λ is the radiation wavelength (μm), and g is the mask-resist gap (μm). Practical control of resist profiles is limited to cases where the values of Q is greater than 3.

Figure 2-21 shows the lateral intensity profile for Q = 3, for two cases of collimation (NQ = 0° divergence). Q = 3 can be achieved with an infinate combination of the parameters W, λ, and g, but a relevant set for the GaAs FETs is W = 0.7 μm, λ = 210 nm and g = 0.52 μm. The normalized exposure profile, $\frac{1}{\Phi}\left(\frac{\partial \Phi}{\partial x}\right)$, is to a first order represented by a straight line with a slope of 3.21 μm^{-1}. The gradient in the exposure profile degrades the resultant resist profile from the ideal vertical edge to a smeared form as shown in figure 2-22. An extensive discussion of deep UV resist characteristics and the factors governing achievable linewidths and resist profiles is included in Appendix E.

* J.G. Skinner, "Some Relative Merits of Contact, Near-Contact and Projection-Printing," Proc. Kodak Interface '73, G-35: 53 (1974).

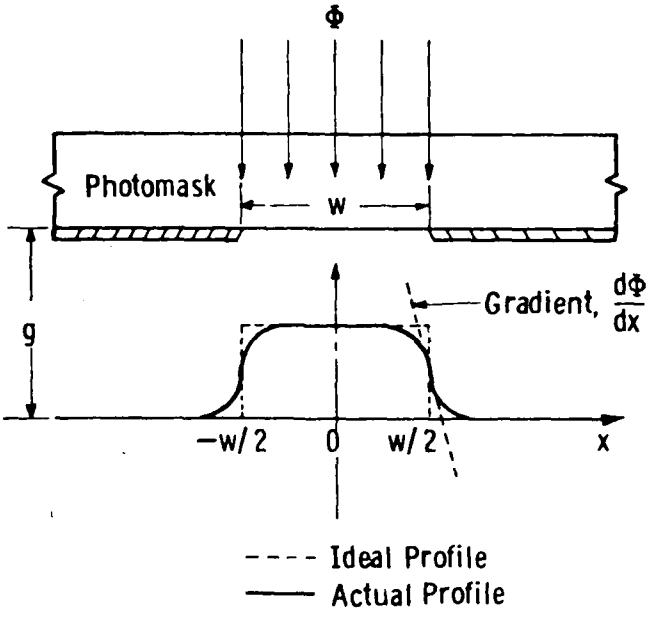


Figure 2-20. Representative Exposure Energy Profiles in the Ideal Case and With Diffraction

2.4.1 Single Layer Techniques

Initial attempts to use lift-off with a deep UV resist for FET gate definition were focused on single layer resists with the emphasis on achieving maximum slope. This approach was used in the belief that deep UV radiation would so improve the edge acuity that satisfactory lift-off would be provided with simple homogeneous single layer resists.

Figure 2-23 shows the results obtained with PMMA exposed at 6.6 J/cm^2. The film thickness was 1.0 μm. The scalloped sides of the bonding pad area are present on the mask and they are the result of individual E-beam scans of the MEBES machine parallel to the gate opening during the photomask exposure. The profile corresponds very closely with that predicted in Appendix E. The rounded upper corner occurs because the gradient in the exposure image, combined with the development process, can attack this area from isotropic directions and the area is exposed to the developer for the total development time. Thr rounded corners were expected to create difficulties during lift-off because they would receive significant metallization which inhibits developer penetration. Figure 2-24 confirms the expected problem as a serious obstacle.

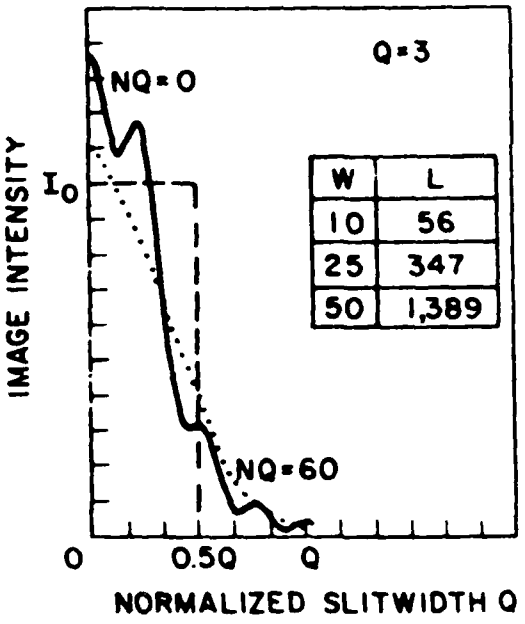


Figure 2-21. Typical Exposure Profile for Q = 3 and Divergence (NQ) of 0 and 60

Dwg. 6409A41

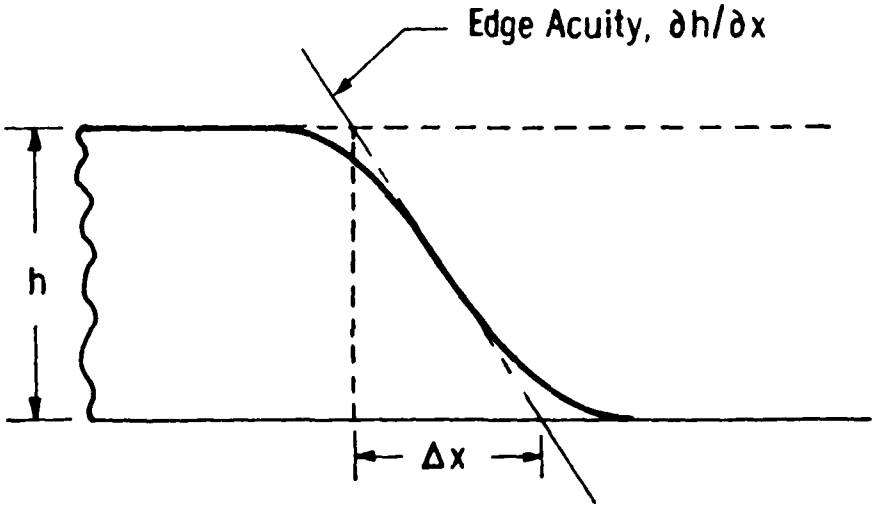


Figure 2-22. First Order Approximation to Resist Image Edge Acuity

The numerous wings of metal around the edges could not be removed even by vigorous ultrasonic agitation, the lift-off yield was low, and PMMA was abandoned as a single layer resist.

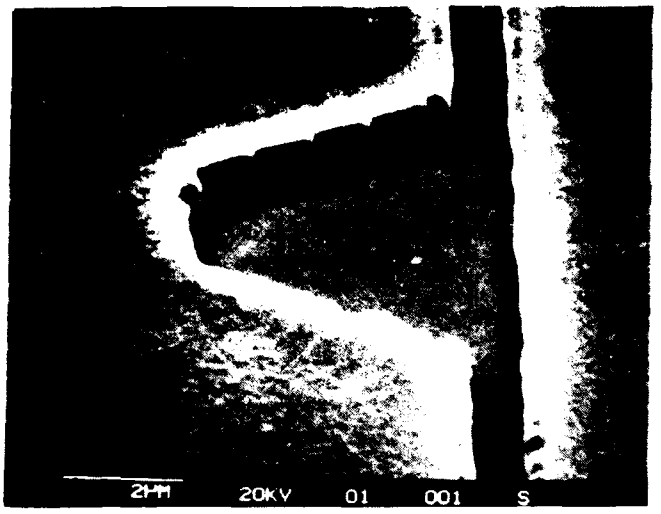
PMIPK, with its higher gamma (contrast factor), should be superior to PMMA in regards to achieving steeper profiles.

Indeed, figure 2-25 shows an improvement greater than that expected due to the increase in γ . Part of the improvement may have been obtained because the photoresist thickness was reduced from 1 μm to only 0.7 μm. Again, however,figure 2-26 shows PMIPK to have wings around the perimeter of the pattern. While PMIPK was superior to PMMA in regards to resolution and edge acuity, it was only marginally better in lift-off performance. PMIPK also experienced severe undercutting during the gate recess etch cycle of the GaAs FETs as a result of low adhesion strength. Further efforts to develop single layer resist images for lift-off were abandoned because: (1) profiles significantly better than that achieved for PMIPK were unlikely, and (2) multilayer technology offered an ideal solution without significant increases in process complexity.

2.4.2 Multilayer Resist Techniques.

Extensive experience with cholorbenzene-soaked AZ1350 photoresist indicated that excellent lift-off characteristics can be achieved if an overhang profile is formed. The problem was to get this profile using deep UV resists. Overhang profiles have been reported by many workers using two-layer resist systems exposed by E-beam systems where the electron backscatter from the substrate produces a pear shaped exposure profile. Frequently, the overhang is naturally achieved by using a low sensitivity (high dose requirement) resist on top of a high sensitivity (low dose requirement) resist. The latter technique appeared most applicable since, unlike E-beam exposures, deep UV exposure profiles are diminished as the substrate is approached due to optical absorption by the resist. A promising multilayer resist system has been reported by Hatzakis. Multilayer systems using P(MMA-MAA) as one of the layers are unique in that the polarity of the two layers can be diametrically opposed. Most polymers are nonpolar in nature and are only soluble in nonpolar solvents such as chlorobenzene, xylene, and toluene. The copolymer P(MMA-MAA) may be polar in nature; in fact, 100 percent methacrylic acid is water-soluble. The copolymer is characteristically

SUBMICRON DEEP UV EXPOSED PMMA IMAGES
THICKNESS = 1μm, EXPOSURE = 6.6 J/cm^2 @ 220 nm



A) GaAs FET gate bonding pad. Scalloped edge on mask due to E-beam raster scan is faithfully replicated.

B) 25,000 X SEM reveals that profile is marginally suitable for lift-off applications.

Figure 2-23. FET Gate Structure Exposed in PMMA Resist

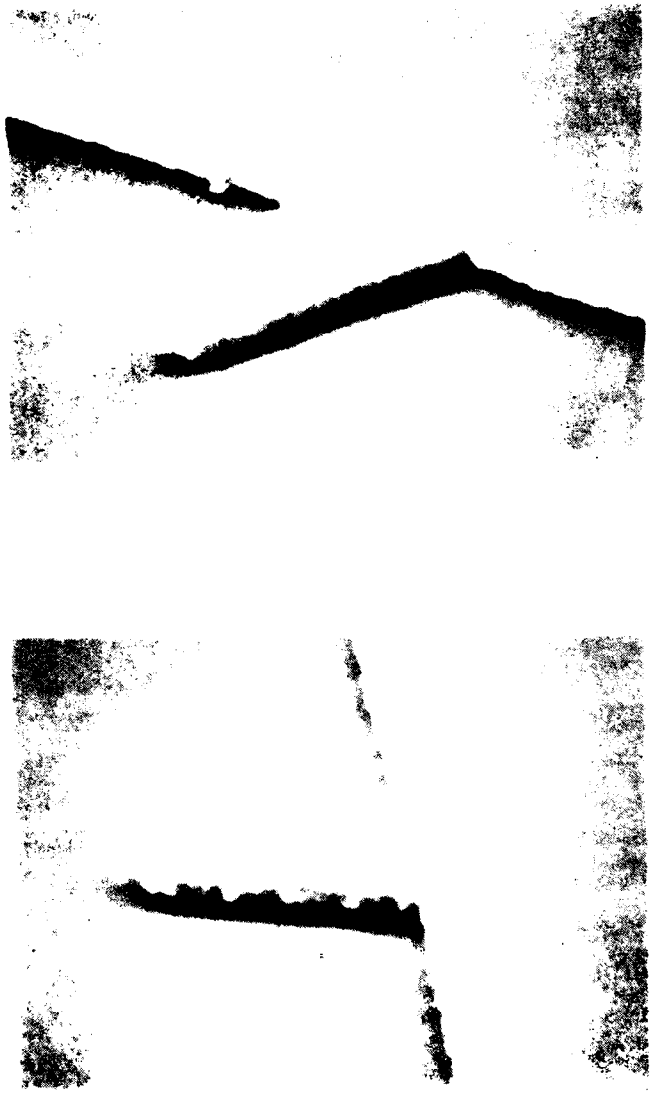


Figure 2-24. Lift-Off Metallization Problems Associated With Rounded Resist Images

PMIPK (ODUR-1010) RESIST IMAGE
THICKNESS = 0.7μm, EXPOSED 110mJ/cm^2 @ 220nm

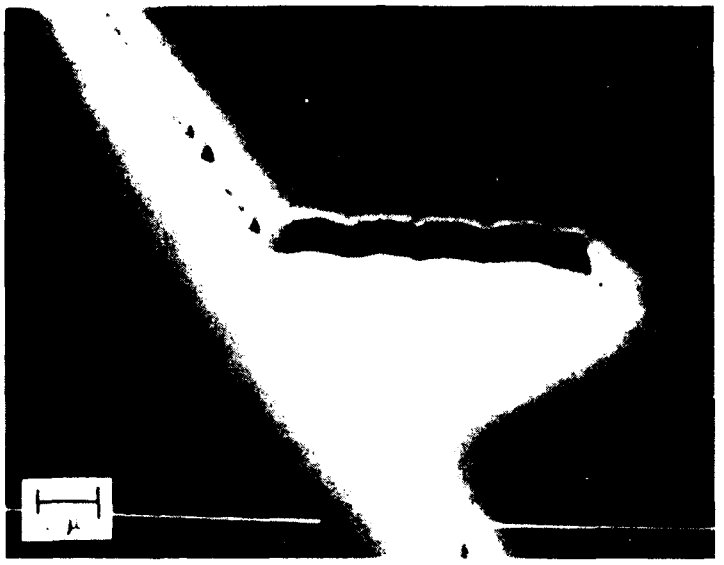
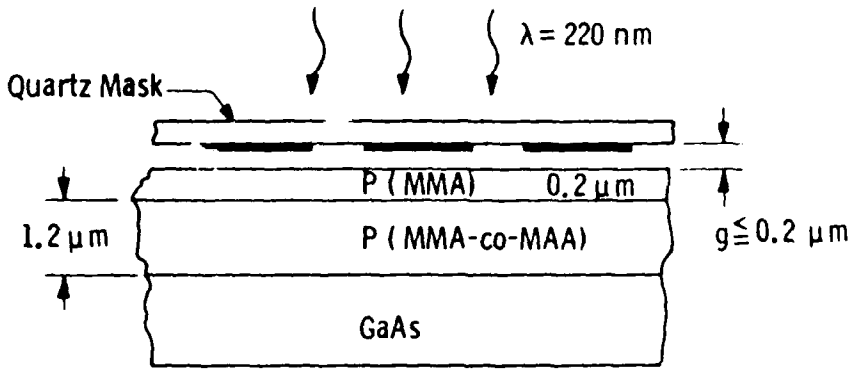


Figure 2-25. Improvement Due to Increase in Contrast Factor Is Readily Apparent for PMIPK Resist

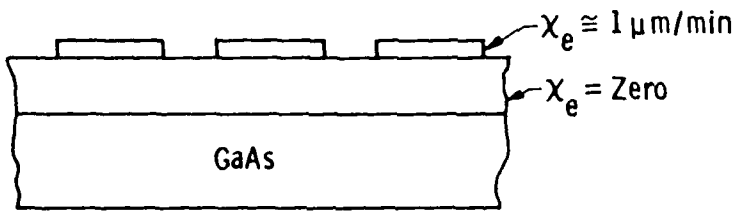
nonpolar in nature for up to 25 percent methacrylic acid. At or above 25 percent MAA, the copolymer is very polar in nature and becomes soluble in acetic acid, ethyl alcohol, and most ethers. The polarity/solvent relationship for both resists is outlined in table 2-5. This combination allows each resist to be developed individually without undo effect on the other resist. The arrangement of the layers and their processing are outlined in figure 2-27. The partially polar MIBK + ETOH developer chosen for PMMA will attack the copolymer layer, but this was not considered a problem because linewidth is controlled by the upper PMMA layer.

Resist images obtained with the PMMA over P(MMA-MAA) bilayer system are shown in figure 2-28. The desired overhang is very evident and sufficient for trouble-free lift-off. A potential problem with adhesion was foreseen, but experiments were necessary with actual device structures to determine the extent of the problem. The lower P(MMA-MAA) layer was expected to have poor adhesion to GaAs due to its polar nature and poor etch resistance, especially to alkaline etches such as were used in the gate recess step. Severe undercutting and attack of the lower resist were indeed observed during the

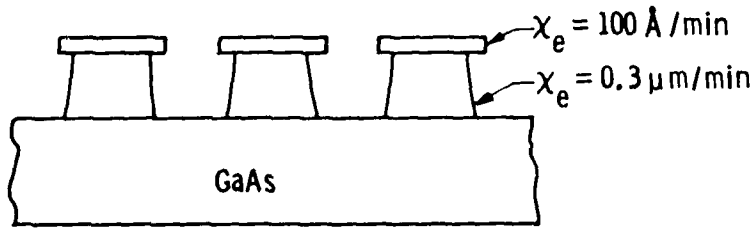
Figure 2-26. Lift-Off Ti-Pt-Au Metallization Patterns Achieved With PMIPK Resist Reveals Wings Less Severe Than With PMMA



Deep UV Expose Bilayer Resist Structure



First (Non Polar) Development – MIBK + ETOH (2.1)



Second (Polar) Development – Ethoxyethanol + IPA (2:1)

Figure 2-27. Structure and Processing of PMMA/P(MMA-co-MAA) Bilevel

DEEP UV LITHOGRAPHY
BILEVEL RESIST TECHNOLOGY
P(MMA)/P(MMA-co-MAA)
0.45 μm / 1.0 μm

0.7 μm gate resist structures ready for lift-off metallization

15,000 X details of overhang in resist profile

Figure 2-28. Multilayer PMMA/P(MMA-co-MAA)
Images Showing Excellent Profiles for Lift-off Technology

gate etch. In addition to this problem, the PMMA experienced cracking during the development of the P(MMA-MAA). Examples of the cracking phenomenon are shown in figure 2-29. The cracks are believed to be due to some swelling of the P(MMA-MAA) during development. Both resists are developed well below their glass transition temperatures and they are very brittle in nature. The PMMA/P(MMA-MAA) structure was abandoned because of the combined poor adhesion and cracking problems.

The bilevel PMMA (high molecular weight) /PMMA (low molecular weight) system was conceived as a possible solution to the two problems experienced with ther PMMA/P(MMA-MAA) system. This system is depicted in figure 2-30 and uses the fact that the sensitivity (dose) of positive type resists decreases with reductions in initial molecular weight. Two versions of this system were conceived. The first conception was based on Esckem PMMA ($\bar{M}_w(0) \approx 1.3 \times 10^6$) over DuPont Eluacite 2041 ($\bar{M}_w(0) \approx 5 \times 10^5$). This approach produces excellent profiles, as shown in figure 2-31a, but lacks flexibility in controlling the amount of overhang due to the limited selection of commercially available PMMA resins. Complete control of $\bar{M}_w$ (0) for the lower layer was provided for by using the procedure shown in figure 2-30. The first flood-type exposure may be varied theoretically to produce any value of $\bar{M}_w$ (0) desired between 950,000 and 0. The results obtained with the double-exposed PMMA/PMMA bilevel technique is shown in figure 2-31b. As expected, this technique experienced no problems during the gate recess etch.

No problems were experienced with the bilevel PMMA/PMMA resist system, but the system is known to be limited by the low glass transition temperature for PMMA ($120^{\circ}C$). Temperatures in this range may be experience during the vacuum deposition of the gate metals, especially the platinum layer, and some flow or droop of the PMMA overhang might occur.

The ideal bilevel resist structure would be P(MMA-MAA)/PMMA, since this structure would have both the excellent adhesion of PMMA and the high glass transition temperature of P(MMA-MAA) for the overhang material. The need for a relatively more sensitive resist in the lower layer than the upper layer was based on simple theory and reports of other workers in the field. Closer consideration reveals this requirement may not be absolutely necessary, even with optical exposures, if sufficient developer sensitivity to polarity can be achieved.

DEEP UV LITHOGRAPHY
BILEVEL RESIST TECHNOLOGY
PMMA/P(MMA-MAA) – 0.4 μm/2.6 μm

15,000 X Positive slope resulting from optical absorption

15,000 X PMMA crack due to swelling of P(MMA-MAA)

Figure 2-29. Multilayer PMMA/P(MMA-co-MAA)
Images Showing Cracks in PMMA Film Due to Swelling of Copolymer

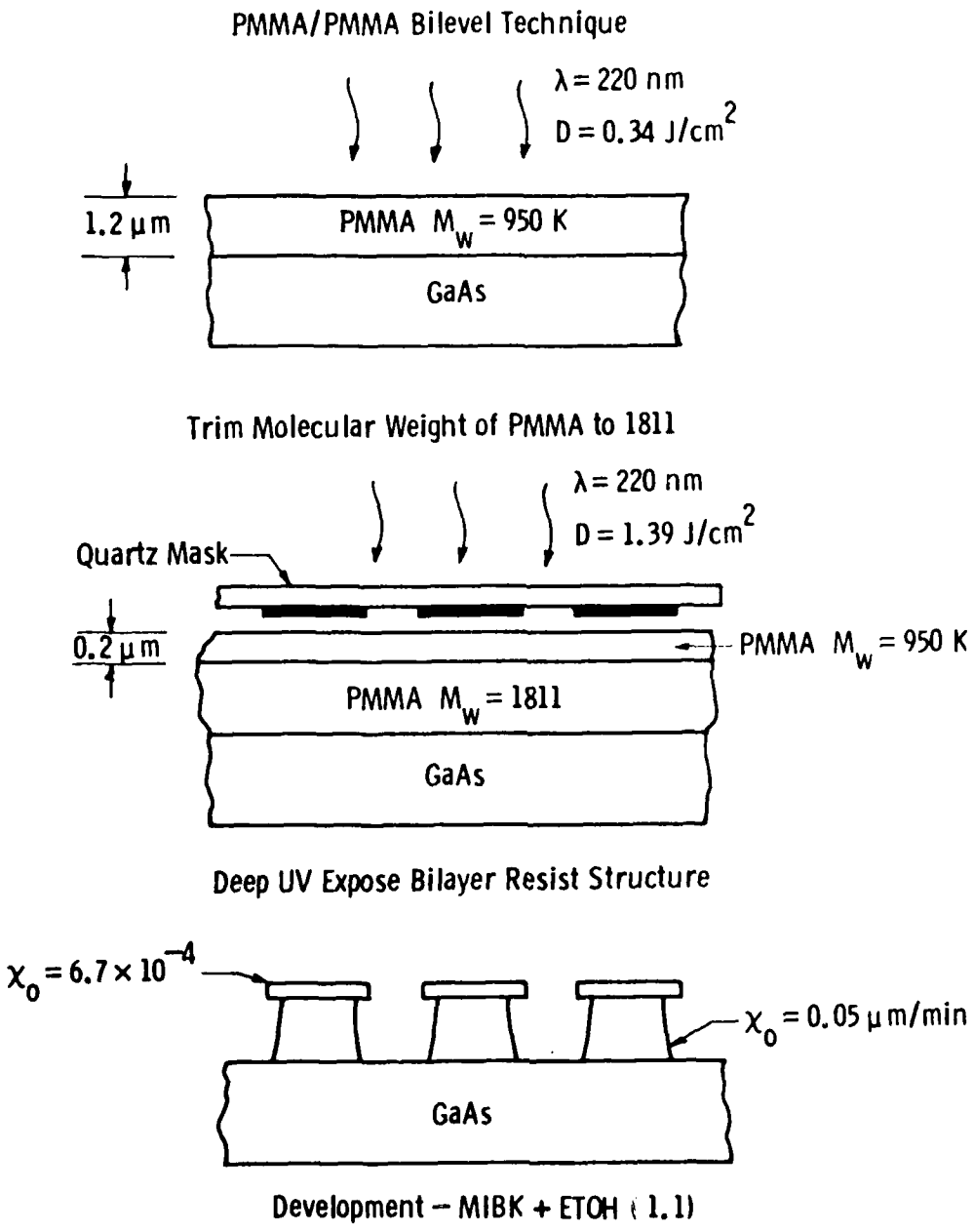


Figure 2-30. Structure and Processing Steps of PMMA (High Mw)/PMMA (Low Mw) Bilevel-Resist System

DEEP UV LITHOGRAPHY
BILEVEL RESIST TECHNOLOGY
PMMA (Hi. $\bar{M}w$)/PMMA (Lo. $\bar{M}w$) – 0.5 μm/1.3 μm

Esschom PMMA/Dupont PMMA

KTI 950K/1.3μm KTI 950K flood exposed 1.39J/cm^2 (30,000 X SEM)

Figure 2-31. Two Bilevel PMMA/PMMA Schemes Were Found to Yield Excellent Overhang Profiles with Excellent Adhesion

Failures in early attemps to produce this inverted sensitivity structure were diagnosed as due to insufficient control of the polarity for the PMMA developer. The choice of ETOH as a nonsolvent to trim the solvent power of MIBK compromises the developer polarity to an extent sufficient to attack the P(MMA-MAA). An obvious solution was to find another combination of solvents/nonsolvents which was nonpolar. A mixture of xylene plus toluene in the ratio of 3:1 was found to be a developer with excellent control of polarity and high sensitivity of dissolution rate as a funciton of exposure. The envisioned new structure is described in figure 2-32.

Pending complete characterization of P(MMA-MAA) and the new developer for PMMA, resist images were obtained to verify the expected qualities. SEM photographs of typical images formed on silicon wafers are shown in figure 2-33. Figure 2-34 shows similar profiles obtained later on GaAs. The images on either GaAs or Si do not show any material problems associated with the reflectivity of the substrate. Complete processing of the copolymer/PMMA images through metallization is not yet complete at this time, but the gate recess etch step has been performed several times with some changes being required in the composition of the etch solution. The standard gate etch solution was alkaline and attached to the copolymer. A weak acid solution appears to have remedied the problem. Figure 2-35 contains an optical photograph (1000X) and an SEM photograph of lift-off metallizations with subsequent removal of the copolymer. The metallization - PMMA distance is indicative of the overlay. Chlorobenzene was used for the PMMA development in these early results and the excess solvent power resulted in severe overhang. This situation is under control with new xylene and toluene developer solution.

The results of our experiments with single layer and bilevel resist systems is summarized in table 2-6. The advantages of the P(MMA-MAA)/PMMA bilevel system are evident when compared with all the other systems. The bilevel copolymer/PMMA system is an excellent system for fabrication of GaAs FET structures, and a set of control curves will be generated to determine the process control necessary for the fabrication of reproducible 0.7- μm gates with high yield.

2.5 DEVICE EVALUATION

In addition to the RF characterization which is used to evaluate the completed monolithic amplifiers and discrete FETs, measurements are made

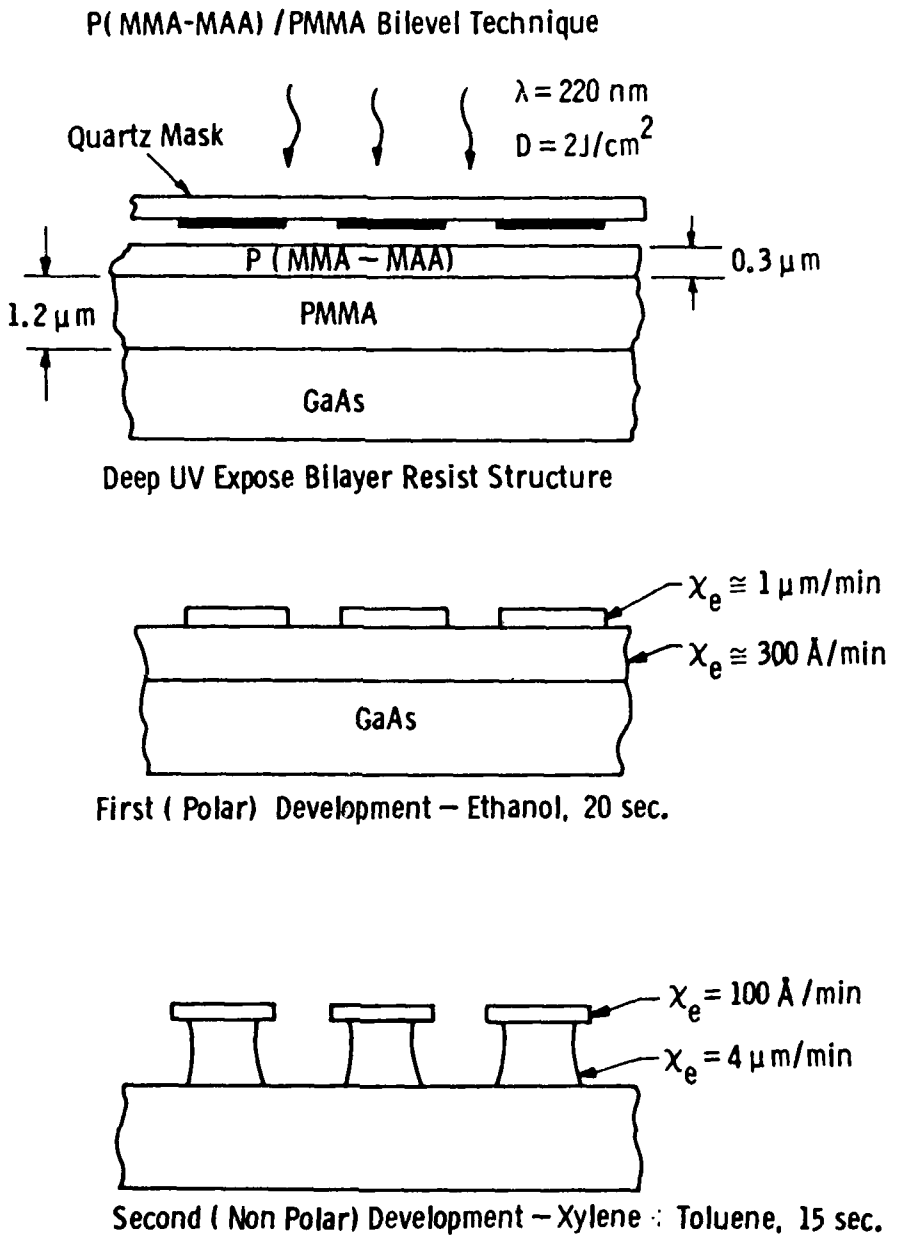
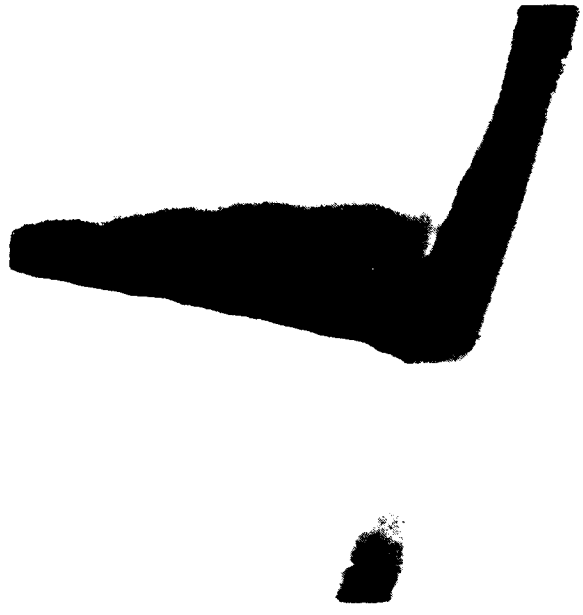
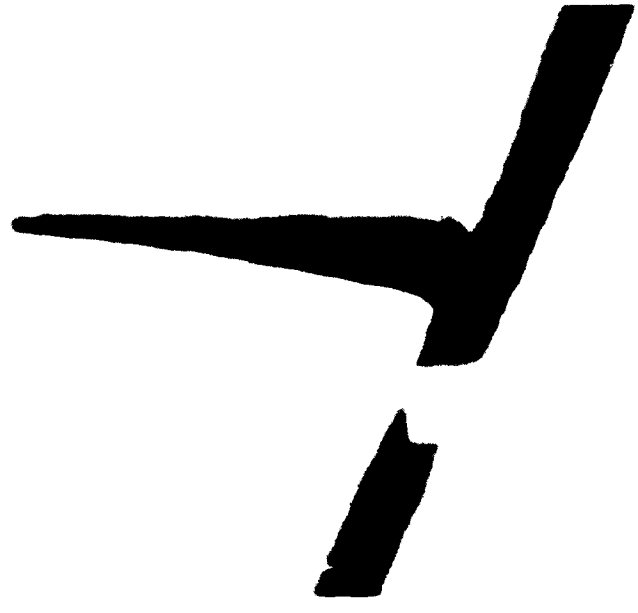


Figure 2-32. P(MMA-co-MMA)/PMMA Bilevel Structure Selected for Process Refinement in Fabricating GaAs FET Devices

DEEP UV LITHOGRAPHY
BILEVEL RESIST TECHNOLOGY FOR LIFT-OFF METALLIZATION
P(MMA-co-MAA)/PMMA – 0.6 μm/1.3 μm



Ideal overhang profile with excellent thermal stability



Line width = 0.62 μm (15,000 X SEM)

Figure 2-33. Bilevel P(MMA-co-MAA) 0.6 μm/PMMA 1.3 μm Images on Silicon Substrate Display Excellent Profiles and Adhesions

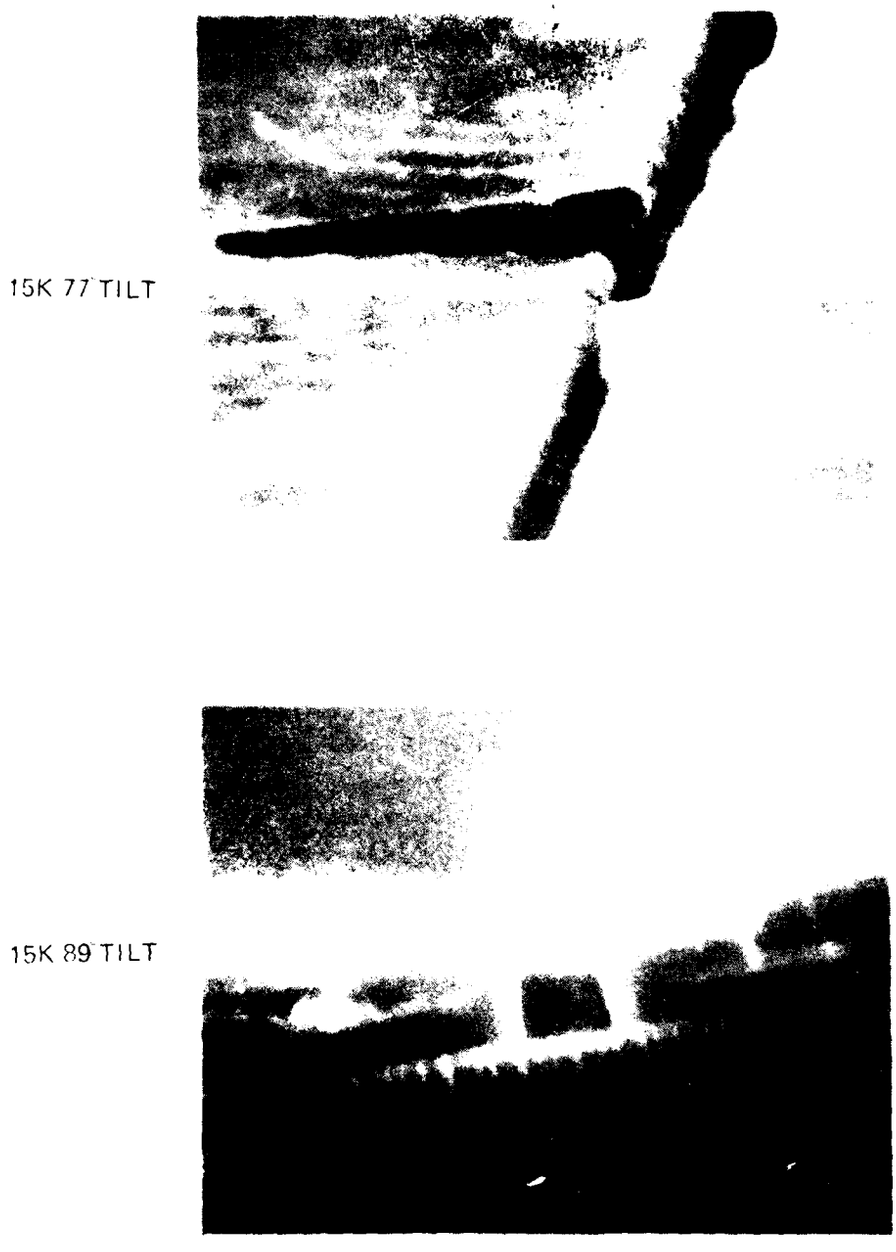
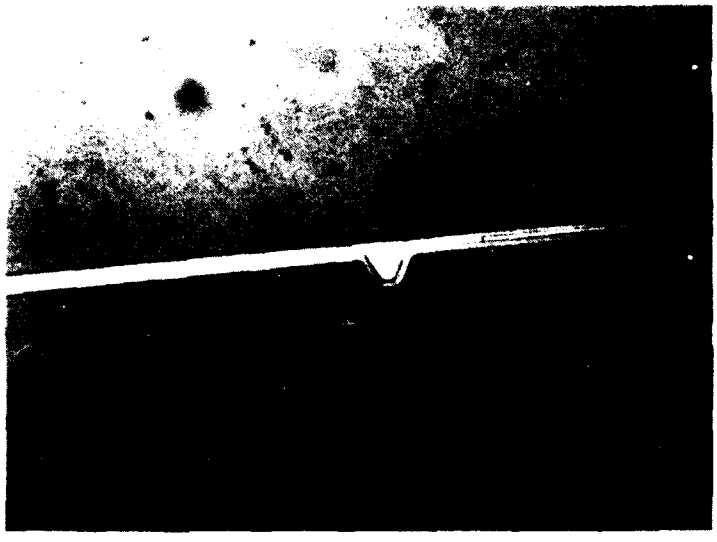


Figure 2-34. Multilayer P(MMA-co-MAA)/PMMA
Images on GaAs Showing Ideal Profiles for Lift-off Metallization

GaAs FET GATE METALLIZATION
BILEVEL RESIST/LIFT-OFF TECHNOLOGY
P(MMA-co-MAA)/PMMA – 0.4 μm/1.4μm
AuGe/Ni/Pt – 1100Å/500Å/400Å



Gate metallization after rejection (PMMA remaining)

P(MMA-co-MAA) overhang = 1.37μm (10,000 X SEM)

Figure 2-35. Lift-off Metallization Performed With Bilevel P(MMA-co-MAA)/PMMA Resist System

during the fabrication process for quality control and process evaluation. The amount of data resulting from these measurements and the final RF measurements is sufficiently large that it is necessary to employ a computer data base and statistical programs for evaluation. The following sections describe the techniques for gathering the data and the statistics employed. A theoretical analysis of the effects of changing FET parameters on amplifiers to be estimated from the expected distribution of processing and material parameters.

2.5.1 Automated Data Measurement System

An important feature of the amplifier development program is the evaluation of the starting material, the process sequence, and the finished device characteristics under dc or low frequency ($\leq 10^6$ Hz) conditions. An automated data measurement system has been used based on the HP 9825 desk-top computer which controls and/or collects data from a Fluke 8502 multimeter, various HPIB controllable power supplies, and a Boonton 1-MHz capacitance meter. Connection to the partially or completely fabricated 2-in. diameter wafers or devices is made with a probe set with up to five probes, each individually controllable with precision micromanipulators. The wafer is moved independently of the probes so that the probes need be configured only once for a given test. Such a system is highly flexible and has been used to measure the implanted carrier concentration and drift mobility as functions of depth, the FET characteristics, and the specific contact resistance of the AuGe/Ni/Pt ohmic contacts. The data from these measurements is recorded on an HP 2000 data cartridge which can then be fed into the data handling system described in the statistics section (2.5.2) shown in figure 2-48.

2.5.1.1 Drift Mobility Measurements

For the drift mobility measurements, an FET is used that has a gate that is very long compared with the source-gate and gate-drain spacing. Such a device has been termed a FATFET in the literature and a cross section of the device is shown in figure 2-36. The Schottky barrier gate is 400 μm long (L) and 200 μm wide (W). The source-gate and gate-drain gaps are each 5 μm. With this geometry, the resistance of the channel under the gate dominates the total source drain resistance and the parasitic resistances of the 5-μm gaps at source and drain are negligible.

In Appendix B, the expression for the drift mobility, μ_d, in terms of the FATFET transconductance, g_m, the depletion layer capacitance, C_g, the

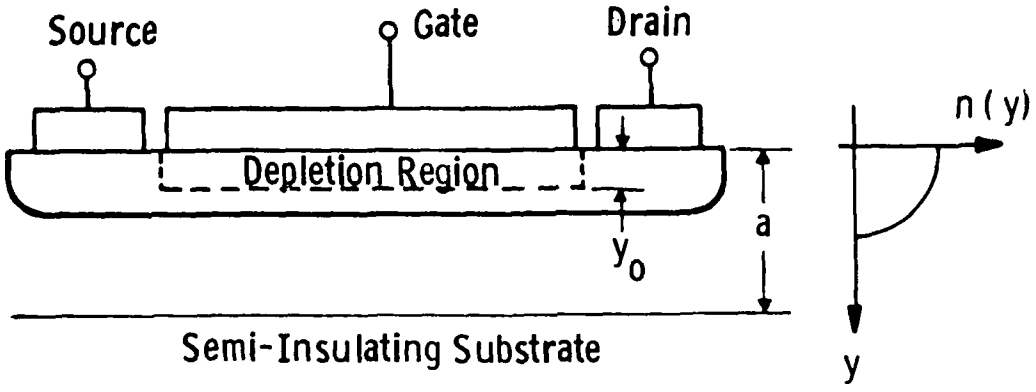


Figure 2-36. FATFET Structure Used in Drift Mobility Measurements

gate length, L, and the source drain voltage, V_{DS}, is derived as

$$\mu_d(y_o) = g_m L^2 / C_g V_{DS}$$

where y_o is the depletion layer depth.

The configuration of the automated data measurement system for mobility evaluation is shown in figure 2-37. It consists of a Boonton 1-MHz capacitance meter and a PAR lock-in amplifier to measure the gate-source capacitance and the drain-source current, respectively. A programmable gate bias power supply controlled by the computer is also included. The sequences of these measurements and data calculation are listed in Appendix B.

2.5.1.2 Results

Test patterns containing long gate FETs were fabricated during runs of monolithic GaAs ICs using Si^{29} implants into undoped, lightly Cr-doped, and heavily Cr-doped substrates. Figure 2-38 shows a plot of drift mobility versus depth into the active layer obtained from measurements of FATFETs fabricated on an undoped substrate. Also shown are plots of the gate-source capacitance, the drain-source current versus the gate bias voltage, and the concentration profile of the active layer. The plot of drift mobility versus the carrier

concentration of the same sample fabricated on an undoped substrate is shown in figure 2-39. The theoretical mobility curves with different compensation ratios and acceptor densities are also shown.

2.5.1.3 Discussion

From figure 2-38 it can be seen that the drift mobility is low near the surface even though the concentration of ionized donors (N_d) remains constant at approximately $10^{17}/cm^3$. This is also true for implants into chromium doped substrates. It is possible that this is due to an increase in the number of acceptors at the surface, which lowers the value of θ, the compensation ratio (N_A^-/N_D^+), from 0.25 to 0.5. This implies a surface acceptor concentration of $5 \times 10^{16}/cm^3$.

As the pinch-off condition is reached in the FATFET, the series resistance of the almost completely depleted channel becomes very high and the reading from the capacitance meter can no longer be simply interpreted as a capacitance value. For the plot shown in figure 2-39, the data are valid at least to the point where the carrier concentration falls to $10^{16}/cm^3$.

The drift mobility of the implanted Si^{29} layer in the undoped substrate is 4400 $cm^2/v\text{-}s$ at 10^{17} cm^{-3} doping density and rises to 4600 $cm^2/v\text{-}s$ at 10^{16} cm^{-3}. the 4400 $cm^2/v\text{-}s$ mobility at 10^{17} cm^{-3} doping is in reasonable agreement with measured Hall mobilities of about 5000 $cm^2/v\text{-}sec$ due to the 10-12 percent difference expected at the magnetic fields used in our Hall setup. The FATFET test structure has provided a continuing monitor of the performance of the Si_3N_4-capped ion implant process.

2.5.1.4 Fet Characterization

The object of this development was to produce a measurement system and software capable of probing FETs on a wafer and transferring a number of key parameters that describe the FET performance to a data bank. Such measurements supplement the more traditional curve-tracer method of obtaining data.

The equipment configuration for these measurements is shown in figure 2-40. It consists of the Hewlett-Packard 9825 computer, two programmed power supplies, and a digital multimeter connected to a manual probe station. The gate bias is set to be 1 volt above ground to allow +1 to -20 volts from a unipolar power supply. The drain bias is connected to a fluke multimeter to allow drain current measurement. The fluke multimeter is a sophisticated instrument that provides features such as remembering peak values. The program makes

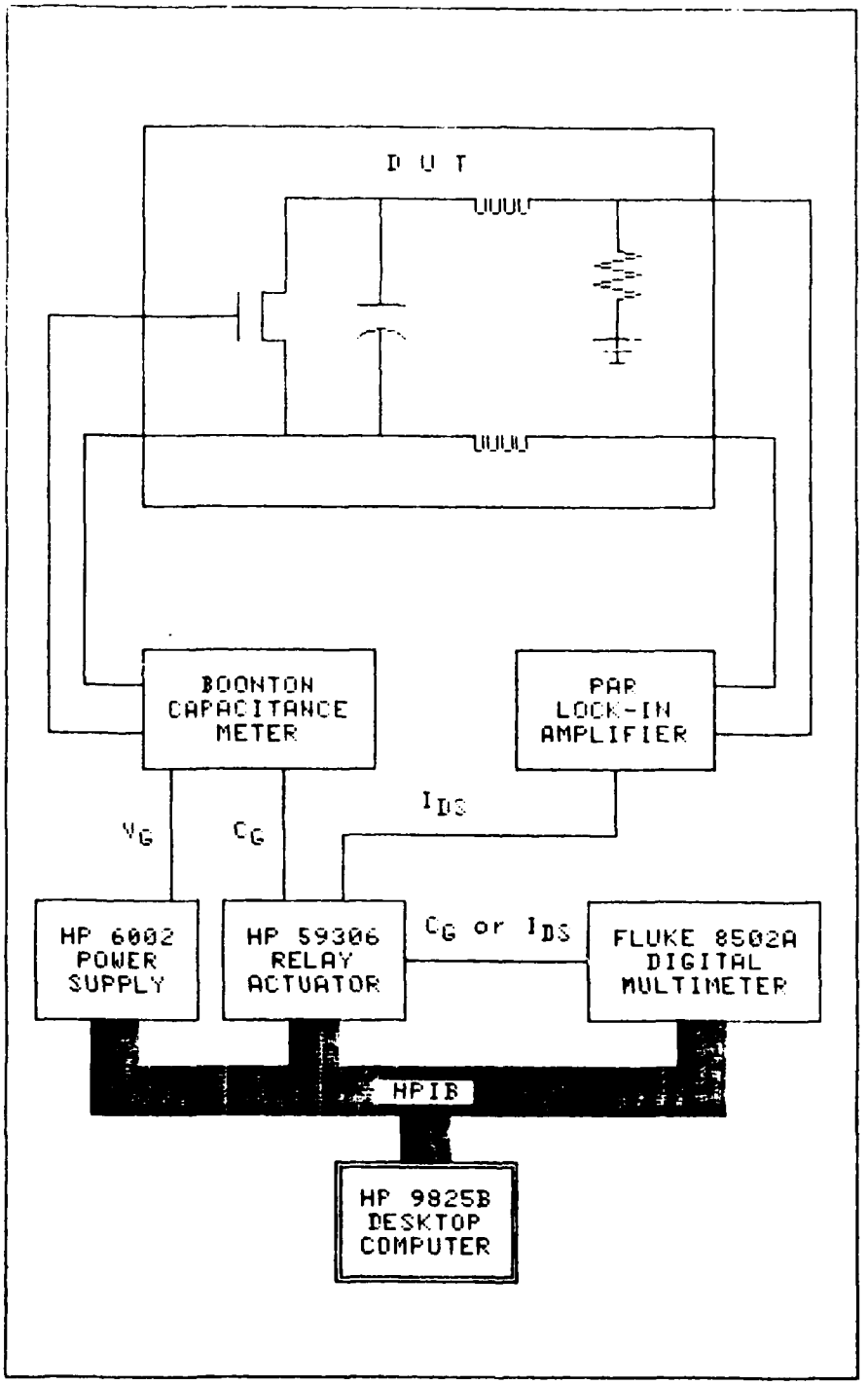


Figure 2-37. Automated Data Measurement System for Mobility Evaluation

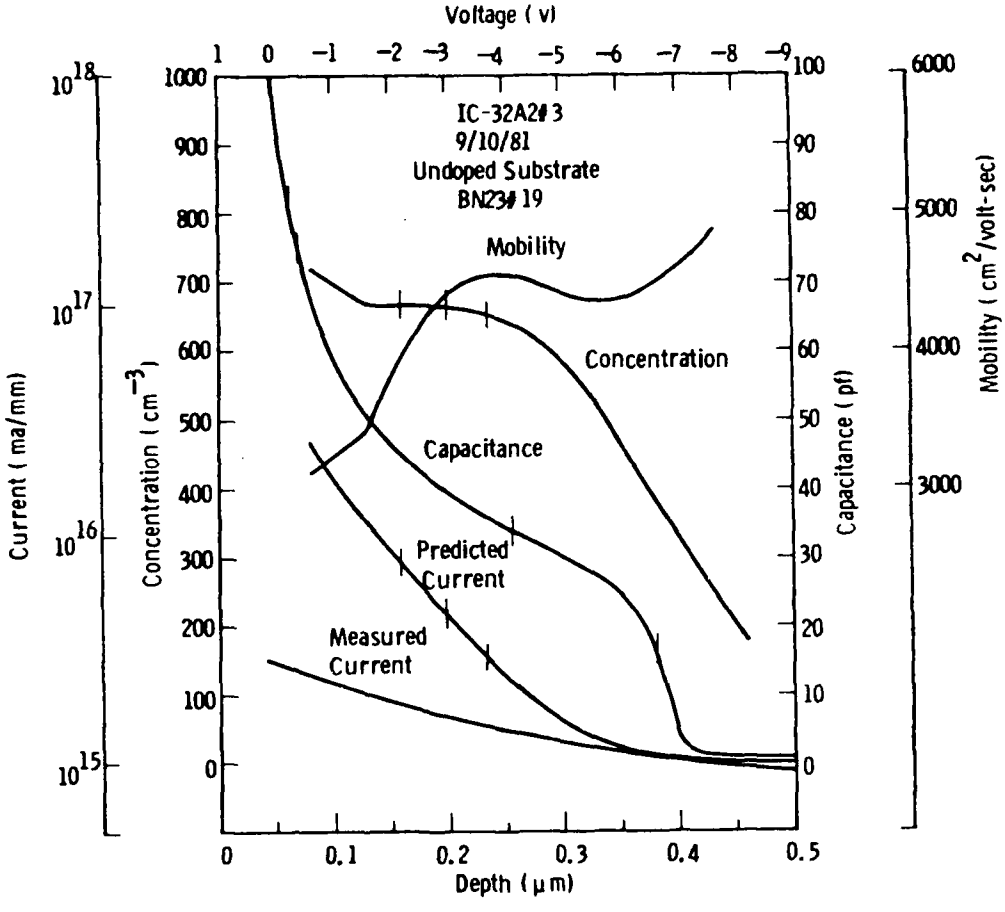


Figure 2-38. Carrier Concentration, Drift Mobility, and Predicted Saturation Current From C-V Data

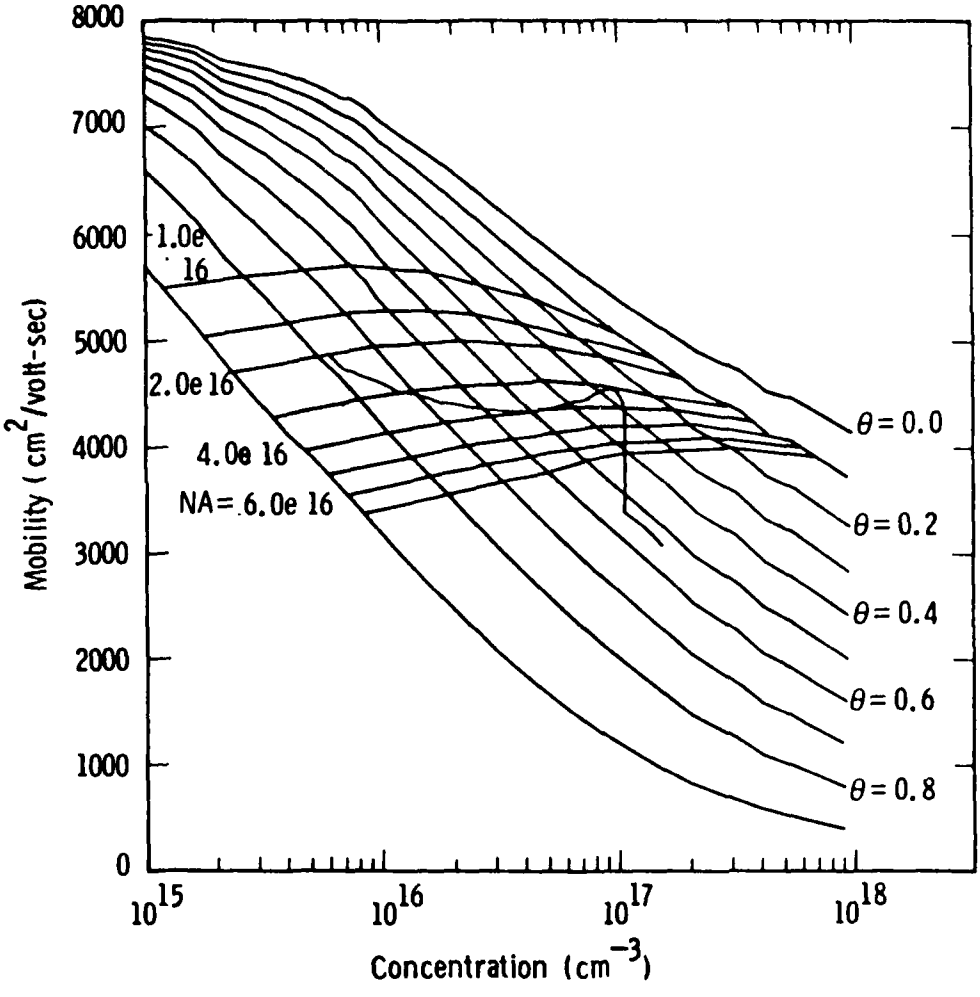


Figure 2-39. Drift Mobility as a Function of Carrier Concentration

approximately 50 measurements per second while controlling the power supplies.The multimeter samples at a faster rate and performs filtering and averaging functions. This equipment completes a measurement sequence in less than 20 seconds. (A faster analog front end will, in the future, reduce this substantially.)

One problem encountered when biasing FETs under probes is that low frequency oscillations can destroy the devices. The FET characterization program limits the range of bias conditions to which the device is subjected and, in addition, monitors maximum gate- and drain- source voltages, maximum drain current, maximum gate-drain voltage, and maximum power dissipation. In addition, the probes are loaded to damp out the oscillations. Figure 2-41 shows a loading of the probes with a 50-ohm resistor between the gate and source and a 1-kilohm resistor in series with a 0.33-microfarad capacitor between drain and source. This configuration was effective in reducing possible oscillations.

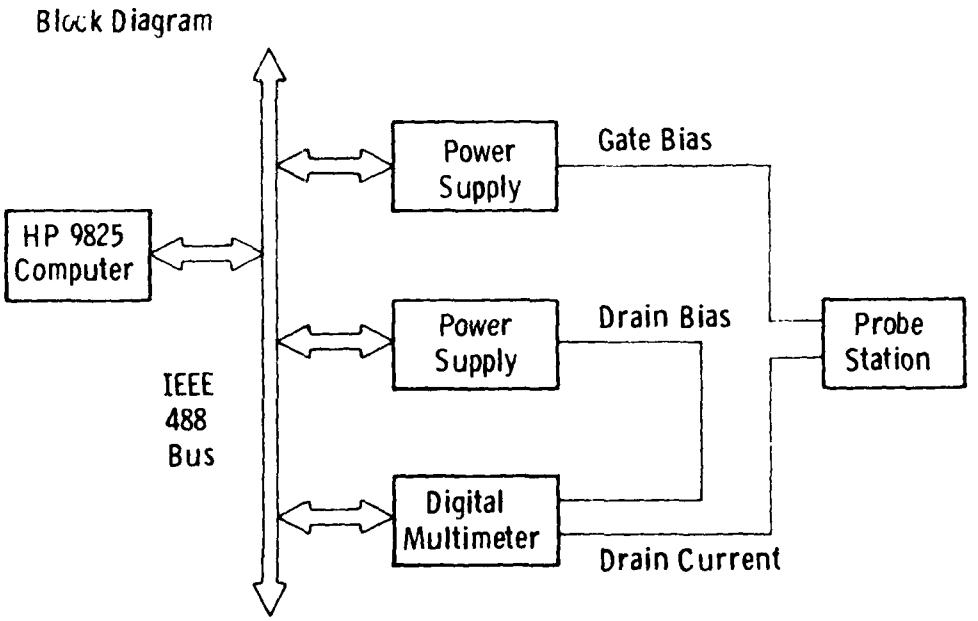


Figure 2-40. FET Characterization Equipment Arrangement

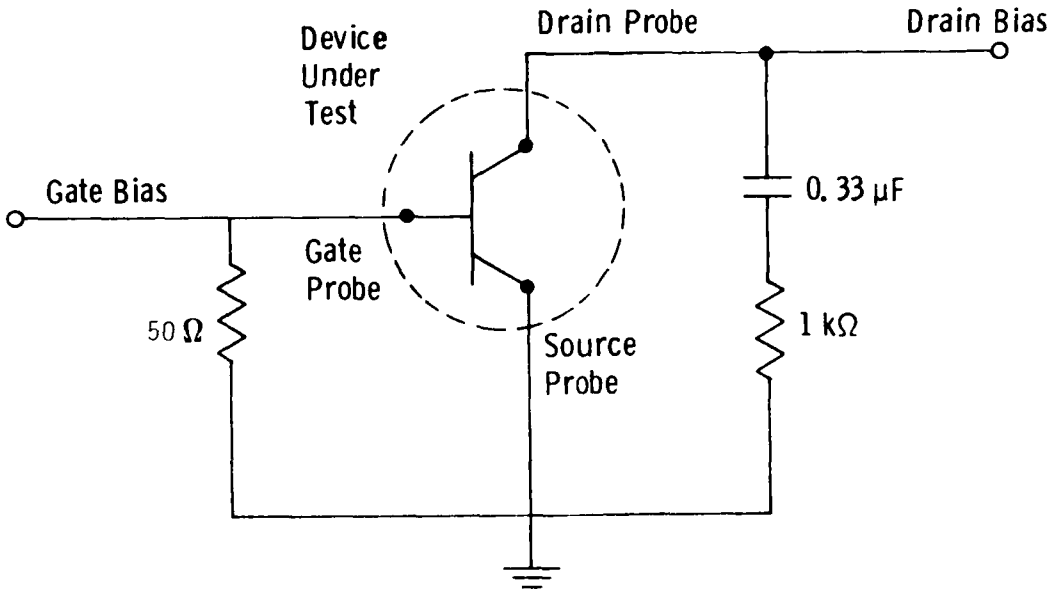


Figure 2-41. Schematic of Probe Loading

The measurement strategy is mapped out in figures 2-42 and 2-43. Starting with gate and drain voltages at zero, the drain voltage is increased in 0.25-volt steps. A straight line is fitted to points 1-4 and its slope is the drain-source resistance in the linear region. The drain voltage is increased until the drain current saturates and the current observed is then I_{dss}. The knee voltage is calculated by multiplying I_{dss} by the drain resistance. The gate bias is now set to +1V to measure full channel current (point 6) and to -1V to measure mutual conductance (point 7). Mutual conductance is defined in this case as the difference in drain current between gate bias voltages of 0V and -1V. The drain current is dropped to a fraction (25-40 percent) of I_{dss} and the drain voltage increased to 5V. As each measurement (points 8-11) is taken, a linear equation is fitted to the data and extrapolated to predict pinch-off voltage. When two successive predictions agree to a close tolerance, the value is accepted. Gate and/or drain voltages are increased beyond pinch-off to find breakdown voltage, which is defined as the voltage at which the drain current rises by 5 percent of its maximum value.

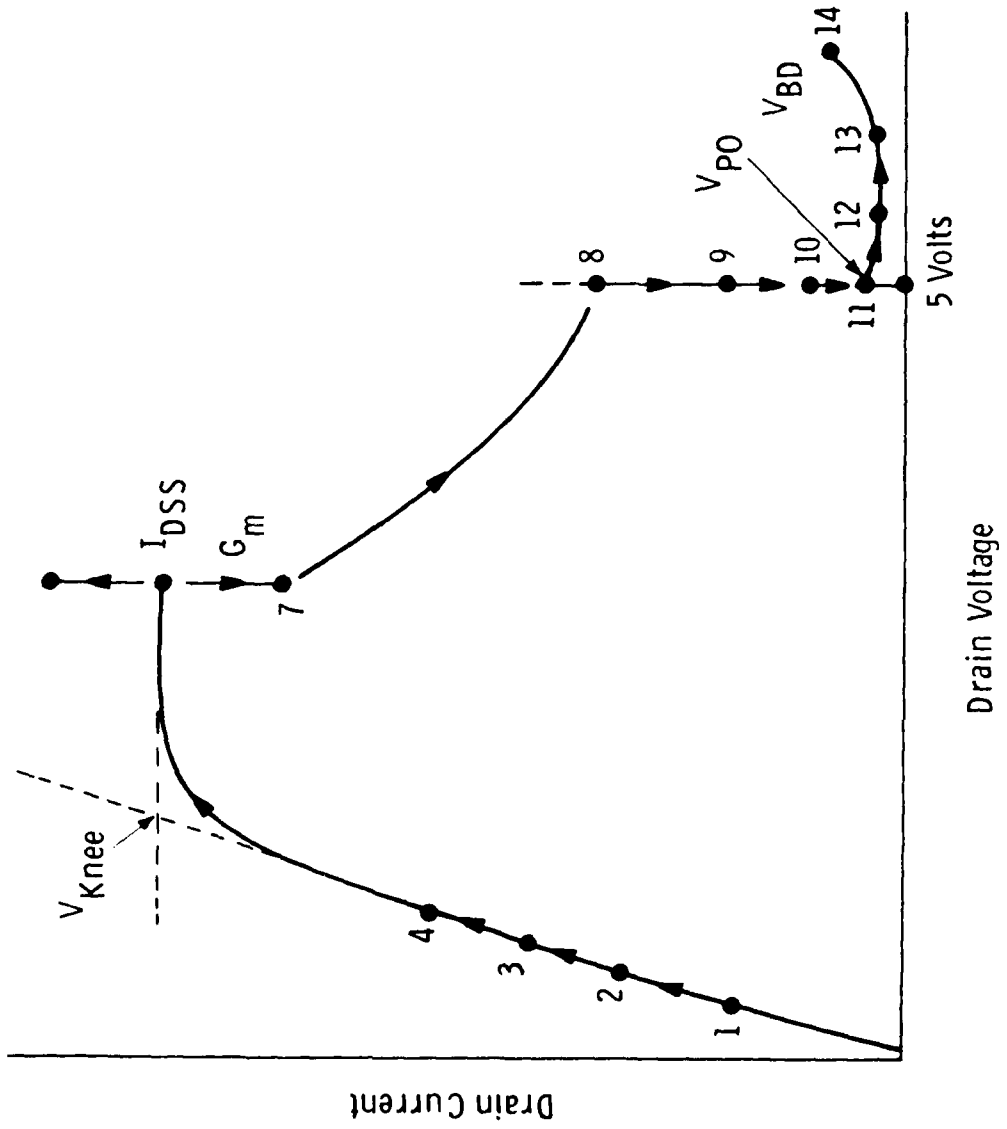


Figure 2-42. Strategy of Determining Device Characteristics

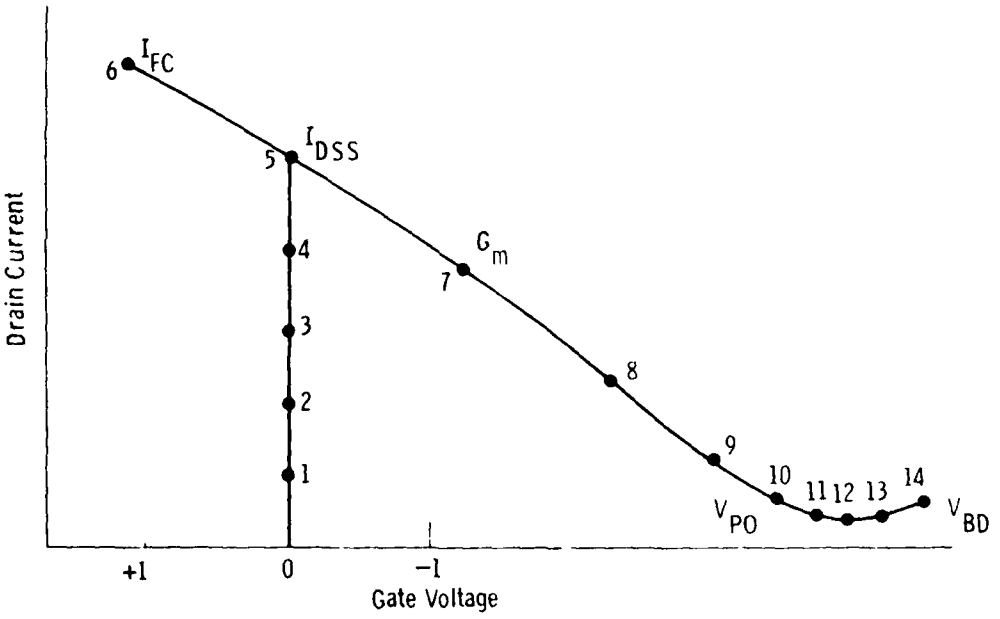


Figure 2-43. Strategy for Determining Pinch-Off Voltage

Data collected in these measurements are transferred in the same way as the mobility data to the data bank (see paragraph 2.5.2).

2.5.1.5 Contact Resistance Characterization

An important part of device processing is the formation of ohmic contacts to the ion-implanted active areas. If the value of the specific contact resistance for the ohmic contacts gets too high ($\sim 10^{-5}\ \Omega\ cm^2$), then the voltage drop that appears at the source and drain contacts of the device can seriously limit the voltage range and, hence, the power output of the device.

As part of the test pattern included on each wafer is a contact resistance pattern that consists of eight identical rectangular ohmic contact pads with different gap spacings between them (see figure 2-44). By applying a constant current across two adjacent pads and measuring the potential difference between them, a plot of voltage drops vs gap spacings can be obtained from each test pattern. An example of such a plot is shown in figure 2-45. A four-point probe method is used to avoid the problems due to probe contact resistance. Gap spacings of each test pattern are measured by a microscope equipped with a digital readout attachment giving a resolution of 0.1 μm.

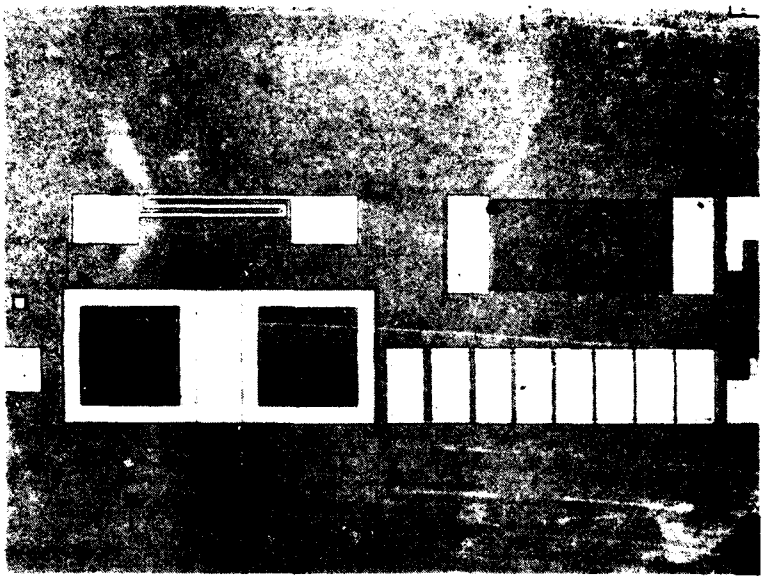


Figure 2-44. Test Pattern Including Specific Contact Resistance Pattern

The configuration of the automated data acquisition system for contact resistance measurements is shown in figure 2-46. Measurements of the specific contact resistance and sheet resistance across a 3-in. wafer of GaAs are shown in figures 2-47 and 2-48, respectively. The value of contact resistance of 1.5 x 10^{-6} $\Omega\,cm^2$ is quite satisfactory for power devices.

2.5.2 Statistical Evaluation

Since the object of this program is to develop an 8 - 12 GHz monolithic GaAs amplifier capable of delivering up to 3 watts of RF power, it is useful to identify those FET parameters which optimize the power output. In order to do this, we have employed a data analysis program called BMDP. With this program, we can look at correlations between the power of GaAs FETs and a number of device parameters or with combinations of those device parameters. In addition, we have used a technique called stepwise multiple regression to look at the most significant correlations in their order of significance. A part of this evaluation has been setting up a data base of material and device parameters obtained from the many fabrication runs performed on this and earlier programs. To date, the data base has over 5600 entries.

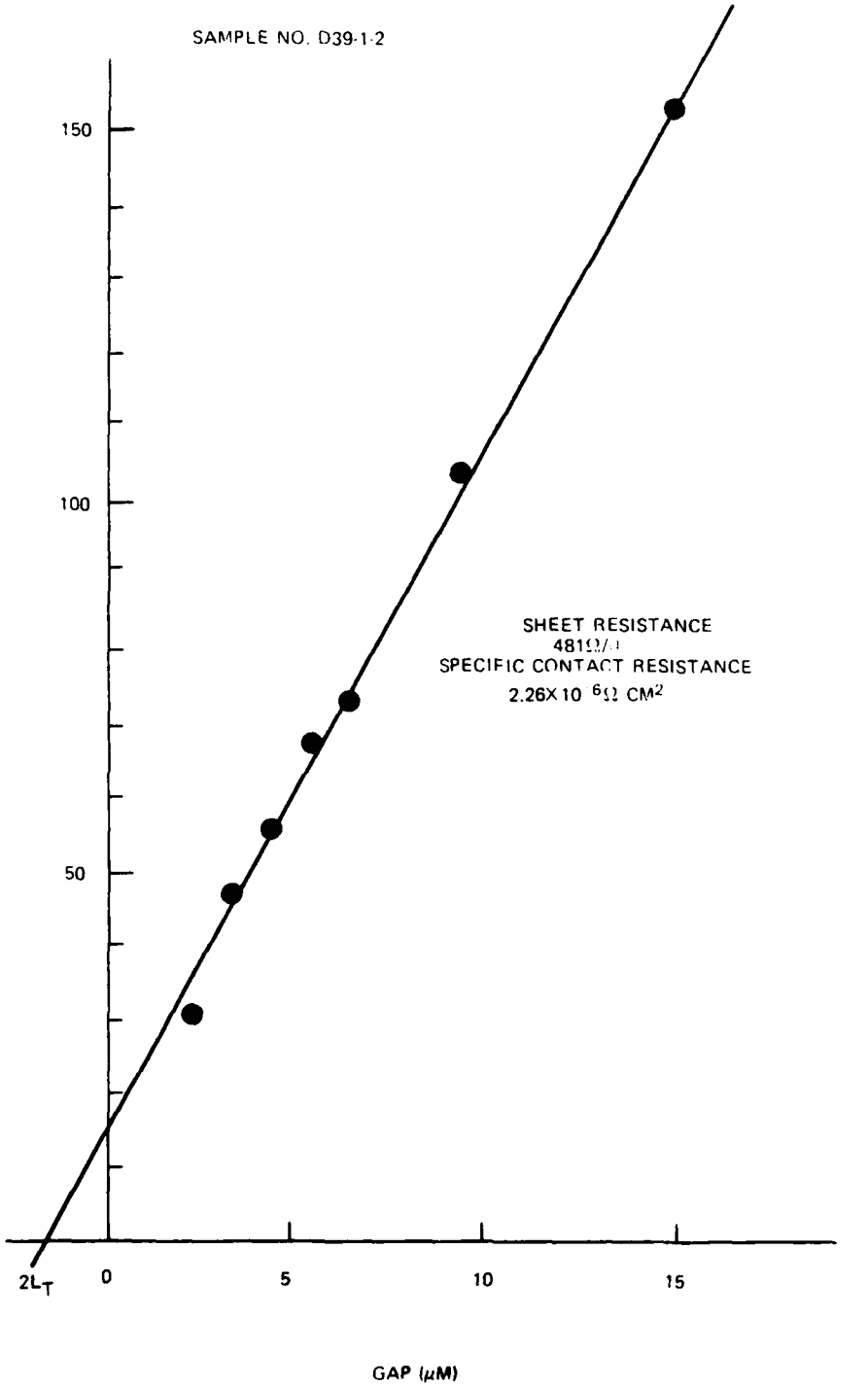


Figure 2-45. Sheet and Specific Contact Resistance

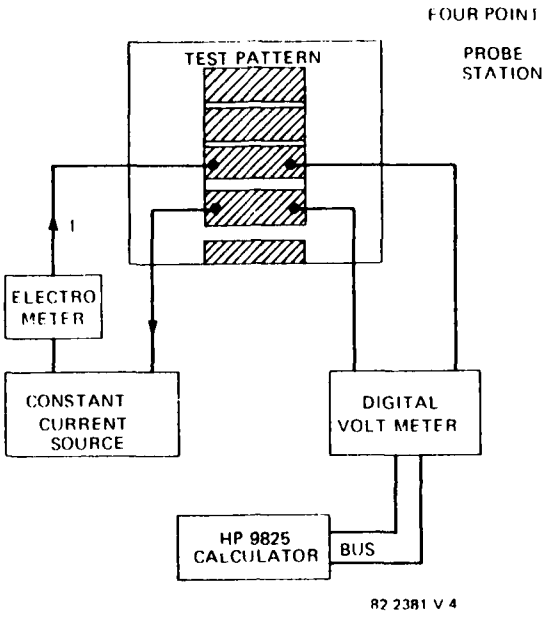


Figure 2-46. Measurement of Contact Resistance

At the end of this section, we include a theoretical analysis of the RF yield of two-stage amplifiers when various FET and circuit parameters are varied with gaussian distributions.

2.5.2.1 Data Base

The Univac Data Management System (DMS) was used to implement an on-line data base because it is a very powerful software package. Some difficulty was experienced because it is a business-oriented system and does not handle scientific data (floating point numbers) easily. It has extensive data retrieval and report generation facilities and can be interfaced to FORTRAN, PL/M, and COBOL programs. We use a three level heirarchial structure to store data on runs (implant data), wafers (material and process data), and devices (geometry and performance data). Over 60 variables are stored, including measurements, small signal gain, equivalent circuit model parameters, power performance, and test conditions. Procedures have been written to enter data from terminals, to transfer data from the laboratory computer to the UNIVAC, and to extract data for analysis. For example, the lab computer, after making a small signal microwave measurement, can send the data to a FORTRAN modelling

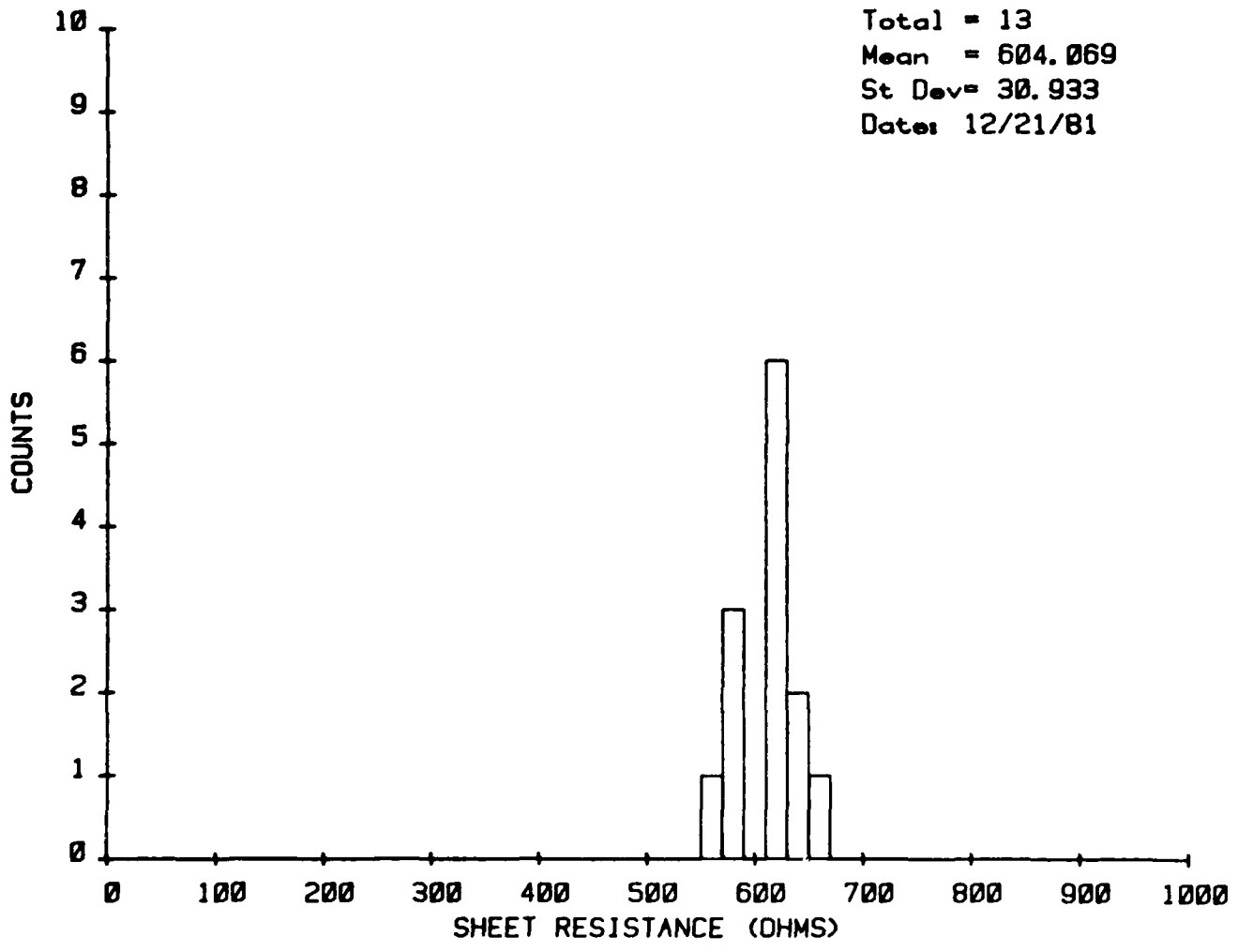


Figure 2-47. Distribution of Sheet Resistance (CD4 (BN 30-45))

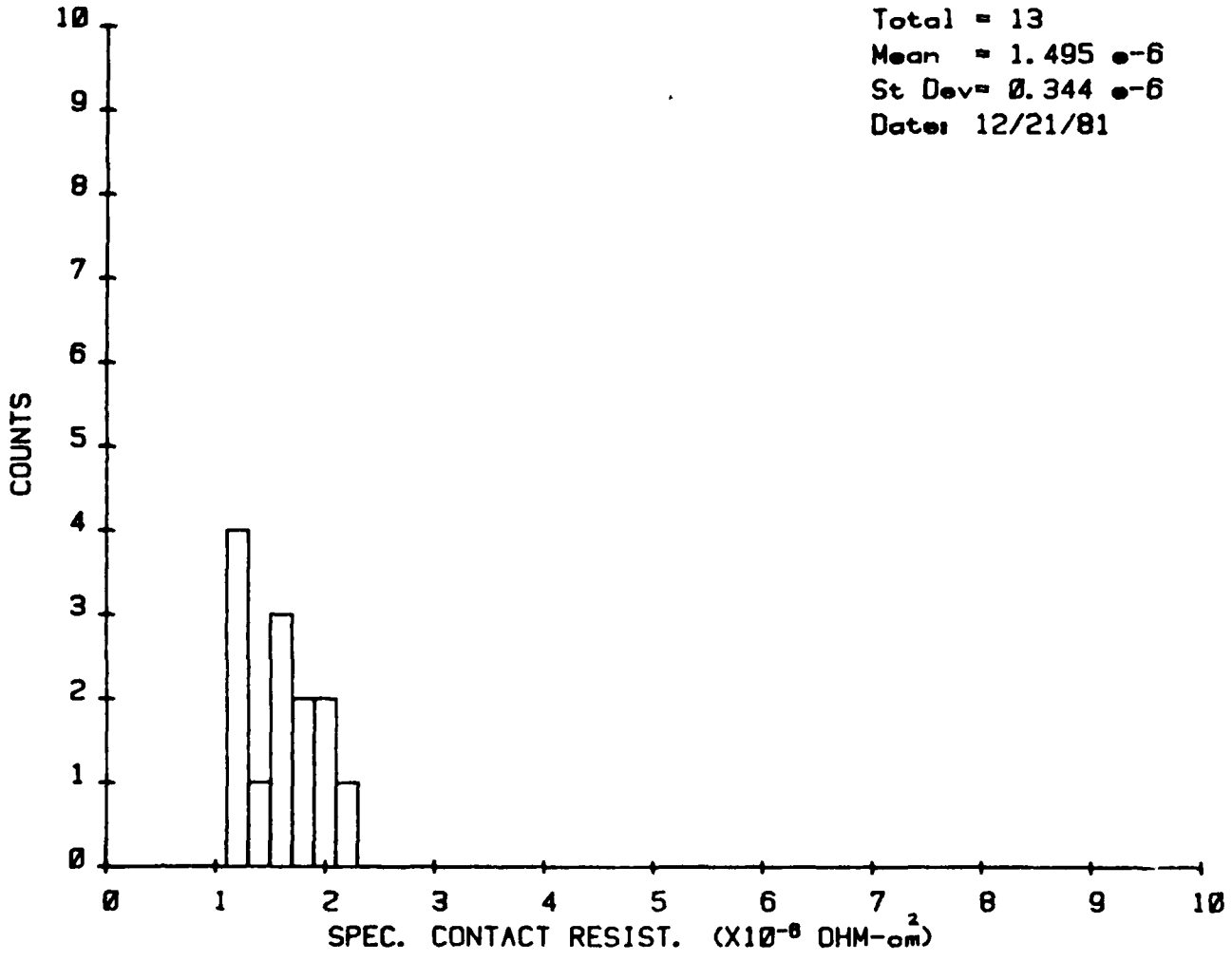


Figure 2-48. Distribution of Specific Contact Resistance (CD 4 (BN 30-45))

program on the UNIVAC. The results are automatically added to a file for input to the data base. This procedure reduces key punching time and eliminates human errors. Our recent purchase of the SUPERCOMPACT[2] microwave circuit analysis program is now being used to do more sophisticated modelling, and the same automatic transfer procedures used between the lab and the DEC VAX 11/780 computer that runs SUPERCOMPACT. A block diagram of the interconnections between the measurement apparatus and the various computers is shown in figure 2-49.

The data base system performs the data entry, editing, and report generating functions. The data is reformatted and written to a file for input to the analysis software.

a. Statistical Analysis

Data analysis is performed by the BMDP statistical analysis package from UCLA. This package can perform many types of analyses and has proven to be a very capable tool. Information produced by a typical run includes correlations, regressions, estimates of error and statistical significance, and plots of selected variables.

Figure 2-50 shows a correlation matrix for a set of 18 variables. The correlation matrix is a table of the correlation coefficients of each of the 18 variables with each of the other variables arranged in a matrix form. The variables were divided into three groups of six and run separately so the printout would fit an 8.5 by 11 in. piece of paper. Figure 2-51 represents the correlation matrix for the entire data base. An APL program was written that could take this output and reduce it to a printout that lists, by variable, every other variable with a correlation coefficient greater than 0.5 (fairly well correlated). An examination of this output reveals that the variables most highly correlated with the output power of the GaAs FETs are (1) the load-line predicted power, (2) the product of saturated drain-source current (I_{DSS}) and gate recess, (3) I_{DSS} divided by the channel thickness, (4) mutual conductance (G_M) from the small equivalent circuit model, and (5) gate recess.

The relationship between variables needs to be examined in more detail than just a correlation coefficient. This can be seen from plots of the variables. Each plot includes two regression lines, one for Y = f(X) and one for X = f(Y). Figure 2-52 shows how these lines are orthogonal for completely

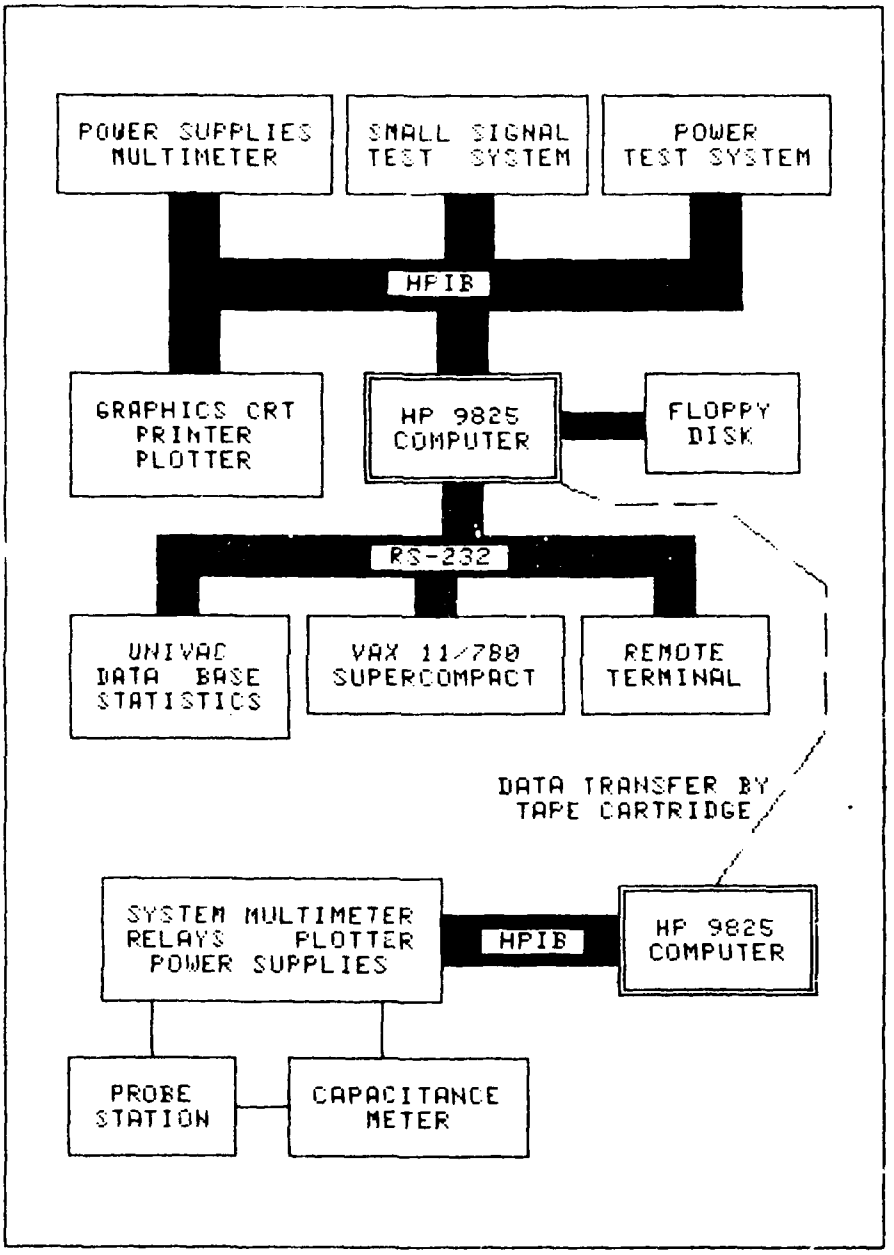


Figure 2-49. Interconnection Between Measurement Apparatus and Data Manipulation Computers

	POWER	POWER GAIN	POWER ADDED EFF	POWER GATE VOLT	POWER DRAIN CURR	PERI-PHERY	MAG AT 4 GHz	MAG AT 8 GHz	MAG AT 12GHz	MSG AT 8 GHz	IDSS
POWER	1.000										
POWGAIN	-.064	1.000									
POWADDEF	.382	.391	1.000								
PGATVOLT	.332	.237	-.184	1.000							
PDRNCURR	.694	.151	-.022	.531	1.000						
PERIPHRY	.025	-.743	-.240	-.272	-.199	1.000					
MAGAT4	-.084	.696	.402	-.074	-.031	-.627	1.000				
MAGAT8	-.122	.590	.498	-.276	-.110	-.521	.765	1.000			
MAGAT12	.109	.712	.536	-.102	.174	-.548	.653	.766	1.000		
MSGAT8	.097	.777	.295	.380	.240	-.693	.620	.494	.559	1.000	
IDSS	.401	.028	.194	-.290	.489	-.089	.167	.119	.216	.034	1.000
VPO	-.112	.143	-.054	.517	-.154	-.221	.098	.022	-.092	.250	-.627

	POWER	POWER GAIN	POWER ADDED EFF	POWER GATE VOLT	POWER DRAIN CURR	PERI-PHERY	GATE RECES	ACTIV ATION EFF	PEAK CONC DEPTH	DC GM	RF GM
POWER	1.000										
POWGAIN	-.064	1.000									
POWADDEF	.382	.391	1.000								
PGATVOLT	.332	.237	-.184	1.000							
PDRNCURR	.694	.151	-.022	.531	1.000						
PERIPHRY	.025	-.743	-.240	-.272	-.199	1.000					
GATERECS	.364	.144	-.037	.664	.249	.090	1.000				
ACTIVEFF	-.006	.395	.578	-.207	-.128	-.147	-.282	1.000			
PKCNDEPT	.028	-.166	-.288	.225	-.015	.161	.518	-.630	1.000		
DCGM	.331	.204	.160	.346	.259	-.246	.447	-.420	.361	1.000	
RFGM	.480	-.123	-.048	.285	.487	-.020	.291	-.371	.053	.565	1.000
LSP	-.054	-.617	-.153	-.337	-.212	.569	-.332	.231	-.135	-.504	-.107

	MAG AT 4 GHz	MAG AT 8 GHz	MAG AT 12GHz	MSG AT 8 GHz	IDSS	VPO	GATE RECES	ACTIV ATION EFF	PEAK CONC DEPTH	DC GM	RF GM
MAGAT4	1.000										
MAGAT8	.765	1.000									
MAGAT12	.653	.766	1.000								
MSGAT8	.620	.494	.559	1.000							
IDSS	.167	.119	.216	.034	1.000						
VPO	.098	.022	-.092	.250	-.627	1.000					
GATERECS	-.091	-.289	-.099	.346	-.189	.338	1.000				
ACTIVEFF	.018	.194	.351	.068	-.099	-.180	-.282	1.000			
PKCNDEPT	-.022	-.177	-.181	.089	-.053	.062	.518	-.630	1.000		
DCGM	.310	.175	.163	.406	.194	.316	.447	-.420	.361	1.000	
RFGM	-.164	-.264	-.063	-.048	.317	.126	.291	-.371	.053	.565	1.000
LSP	-.527	-.379	-.423	-.773	-.067	-.318	-.332	.231	-.135	-.504	-.107

Figure 2-50. Correlation Matrix of 18 Variables

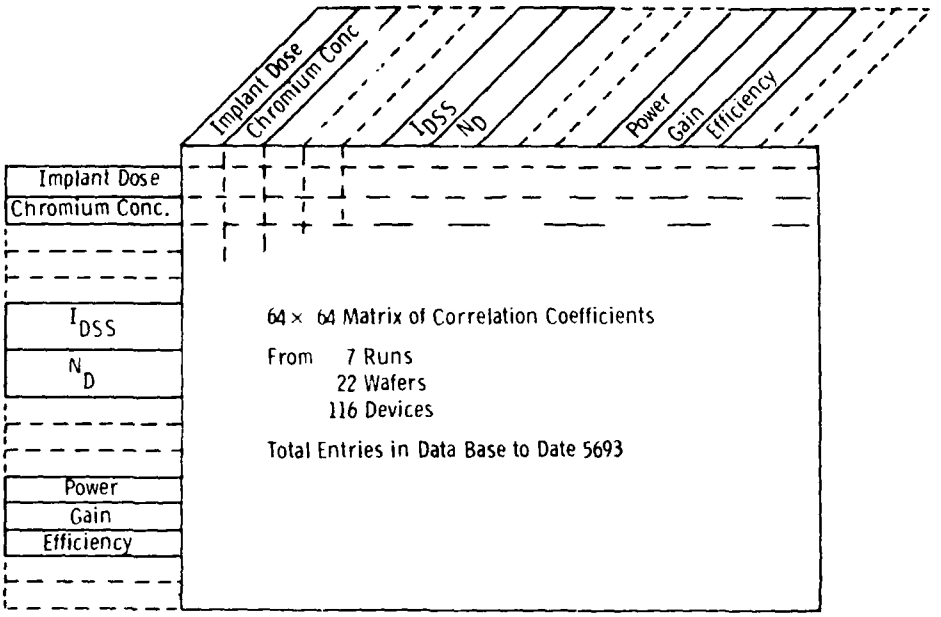


Figure 2-51. Schematic Representation of Correlation Matrix

uncorrelated data, but converge to a single line with correlated data. This behavior arrises from the fact that the least squares fit of a regression line minimizes the vertical (Y = f(X)) or horizontal (X = f(Y)) errors, rather than the errors perpendicular to the fitted line. Figures 2-53 through 2-55 are examples of BMDs bivariate plots. Figures 2-53 and 2-54 show a good linear correlation between the variables. The I_{DSS} and gate recess depth are two of the most highly correlated parameters. The linear correlation coefficient in figure 2-55 relating doping density to output power is not high, but there seems to be a higher order relationship. The broad band indicates that concentration does affect power and that the optimum value for concentration is around 1.35×10^{17} cm^{-3} with an 0.15- μm thick channel. In some cases, the correlation between two variables is controlled by a third or more other variables and, in this case, a more sophisticated technique is required. BMD includes a function called *stepwise multiple regression* (SMR) that can deal with thi problem.

To explain the working of SMR, we will look at those variables which correlated with the RF power output of devices from one of the device runs

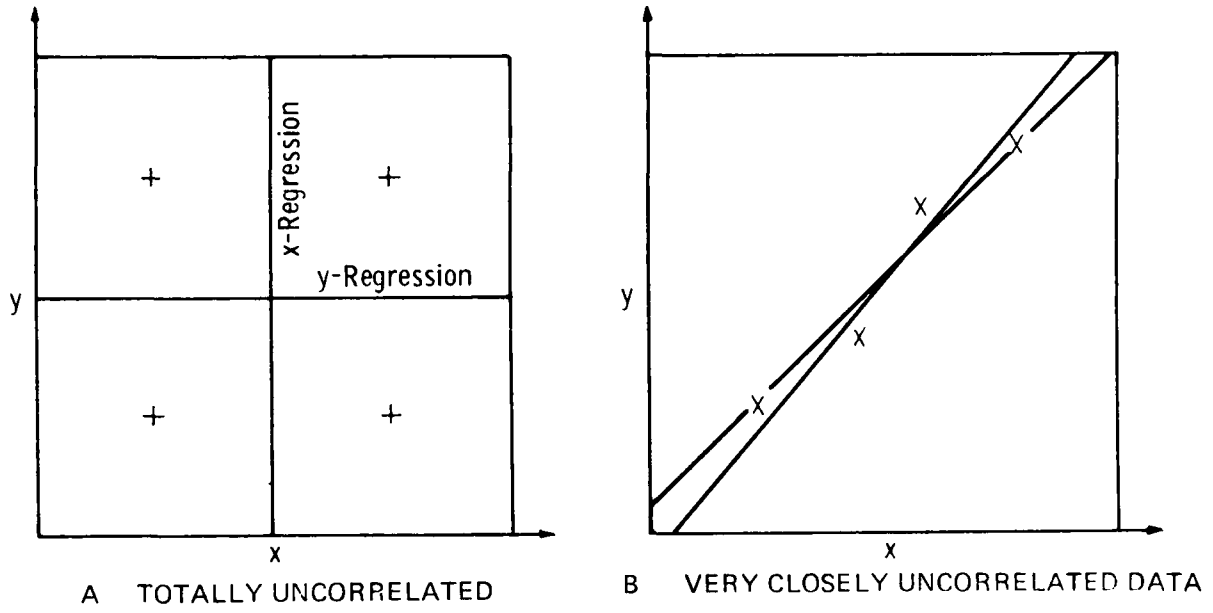


Figure 2-52. Example of X and Y Regression Lines on Uncorrelated and Correlated Data

fabricated during the past year. Several variables which correlate with power are related to or computed from I_{DSS}, but only one of them should properly be included in the regression equation. There are other variables which make a contribution but do not correlate well. The SMR technique generates a set of predictor variables one at a time, at each step picking the variable that correlates best with the unexplained variance, or residual. The first variable selected is predicted power, since it correlates best with the observed power. The predicted power is 1/8 ($2V_{DRAIN}$ x I_{DSS}). Since this expression includes I_{DSS}, the importance of I_{DSS} and related variables now drops substantially and gain-related factors become more important. The next most important variable is now the RF G_M (from the small signal model). Its importance was almost unchanged after the first step where predicted power was removed, indicating that it has a completely independent contribution. The third variable to come to the fore is the deep implant dosage. This variable had the lowest importance of all (correlation of 0.00) in the original list, but now makes a significant contribution. The alogrithm continues, adding gate recess, chromium doping or undoped substrate, pinchoff voltage, and peak

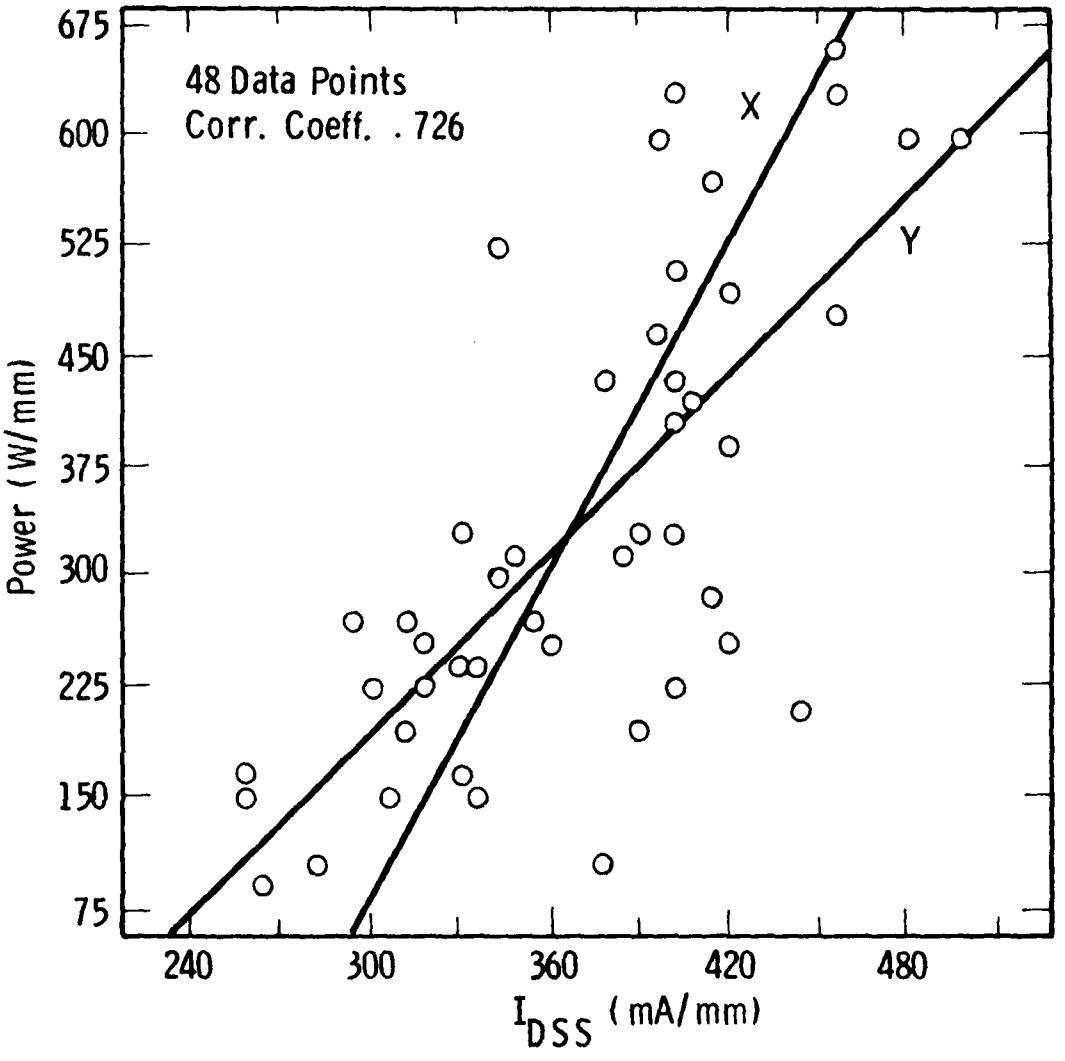


Figure 2-53. Correlation of Power/MM With I_{DSS} For Runs 20, 21, 26, 29 and 31

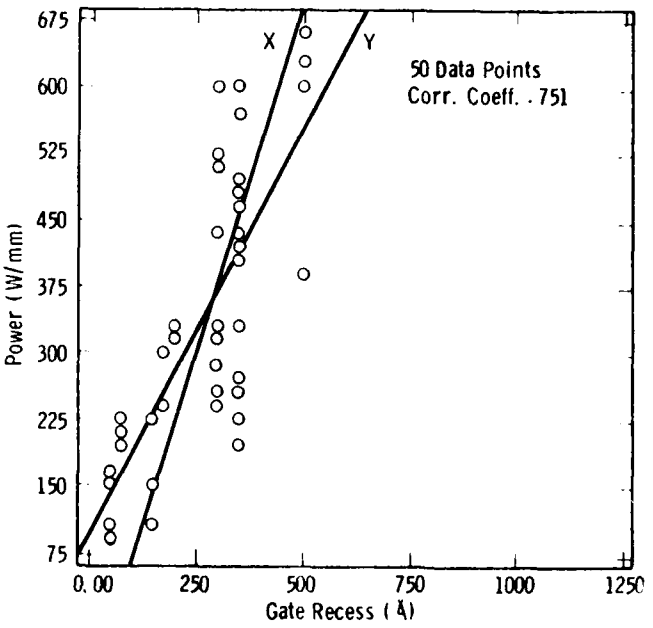


Figure 2-54. Correlation of Power/MM With Gate Recess for Runs 20, 21, 26, 29 and 31

concentration until none of the remaining variables have more than a random correlation. The following table summarizes these results.

Step No.	Variable Entered	Variance Explained Percent	Standard Error mW/mm
1	DC load line prediced power	49.5	114
2	GM from small signal model	65.1	96
3	Deep implant dose	68.2	92
4	Gate recess	73.4	85
5	Chrome doping	76.3	81
6	Pinchoff voltage	79.8	76
7	Peak concentration	82.8	71

The third column lists the amount of variation in power accounted for by the regression at each step. The final result shown (82.8 percent) is reasonably high and we hope to improve on it. The fourth column lists standard

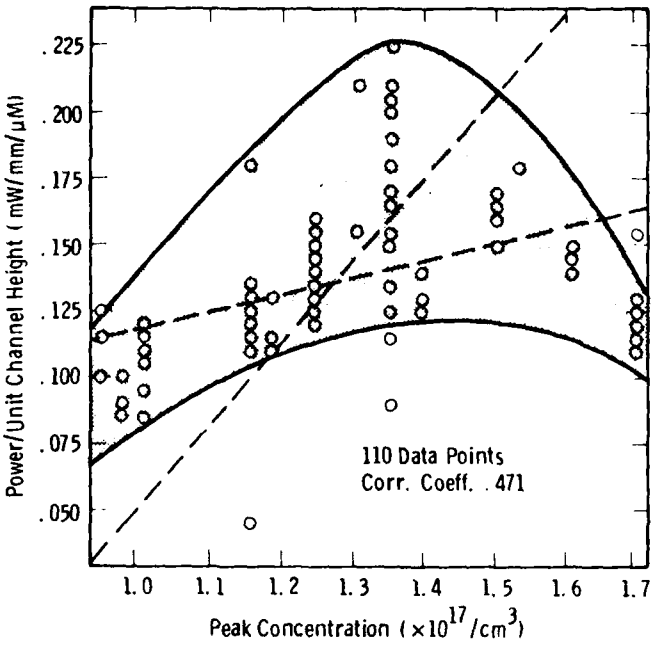


Figure 2-55. Correlation of Power/Unit Channel Height and Peak Carrier Concentration

error. In about 70 percent of the cases observed, the difference between the actual value of output power and the value predicted by the regression is less than the standard error.

The data base is continually expanding as more fabrication runs are completed and evaluated. The automation of data taking has made and will make the collection of data base entries much easier. Routine measurement and storage of device characteristics as a function of position on a complete wafer, such as mobility, full channel current, FET knee voltage and breakdown voltage, are expected to yield data that can be related to material preparation and properties.

2.5.2.2 Statistical Analysis of Manufacturability

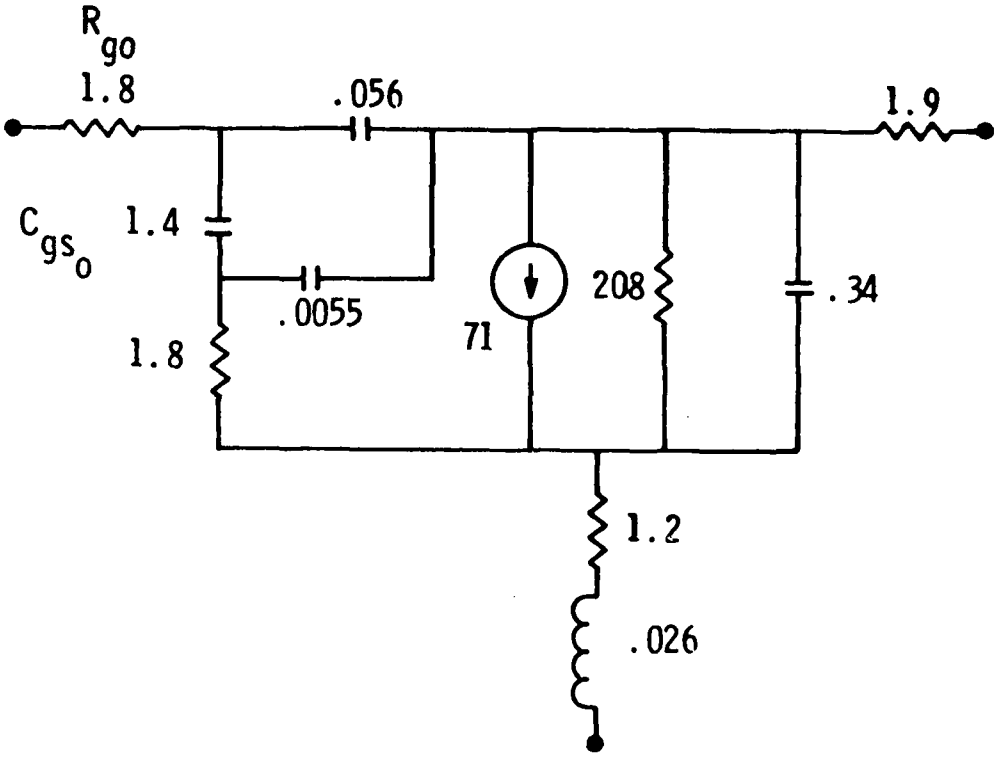
A series of computer studies on the effects of process variations on the RF yield of monolithic amplifiers was undertaken to provide a basis for comparing the manufacturability of alternate circuit designs. This work determined the sensitivity of both the small signal gain characteristics and the large signal power performance to changes in doping density, gate length, and other variables. The effects have been simulated using the lumped element FET model, shown in figure 2-56, along with large signal load-pull characteristics. For the small signal case, the effect of L_G and N_D on the FET parameters can be expressed as:

$$C_{GS} \alpha \left[\frac{L_G}{L_{GO}}\right] \cdot \left[\frac{N_D}{N_{DO}}\right]^{1/2}$$

$$R_G \alpha \left[\frac{L_{GO}}{L_G}\right]$$

where C_{GS} is the gate-source capacitance, R_G is the gate metal resistance, N_D is the doping density in the GaAs, and L_G is the gate length. The second subscript, 0, indicates the original design value of a parameter. For example, L_{GO} represents a nominal design gate length of 1 micrometer. The FET model values in figure 2-56 represent a 1200-μm periphery GaAs power FET. By independently varying gate length, L_G, and doping density, N_D, about their normal values, the FET variations and from them the variations in gain performance of a two-stage GaAs power amplifier were calculated as shown in figure 2-57 by the solid lines. This calculation was performed using the COMPACT[2] microwave circuit analysis program. A 10 percent change in N_D produces almost a 1-dB change in the amplifier gain, while a 10 percent change in L_G changes the gain by 2 dB.

The variation of the power performance (as opposed to the amplifier gain) as either N_D or L_G is altered is a more complicated calculation because the large signal values of the FET model elements are functions of the drive level.[7] This applies most stringently to the FET output elements and simplifying assumption can be made. Since S_{12} of these devices is small, it is valid to treat the GaAs FET as a unilateral device. Therefore, the power performance of the FET is characterized by its load-pull contours for the



- Nominal Gate Length = 1 μm = L_{go}
- Nominal Doping = $1.1 \times 10^{17}/cm^3 = N_{Do}$

- Doping Change: $C_{gs} = C_{gso}(N_D/N_{Do})^{1/2}$
- Gate Length Change: $C_{gs} = C_{gso}(L_g/L_{go})$; $R_g = R_{go}(L_{go}/L_g)$

Figure 2-56. Small Signal Lumped Element Model of 1200-μm Direct Implanted FET in Integrated Circuit

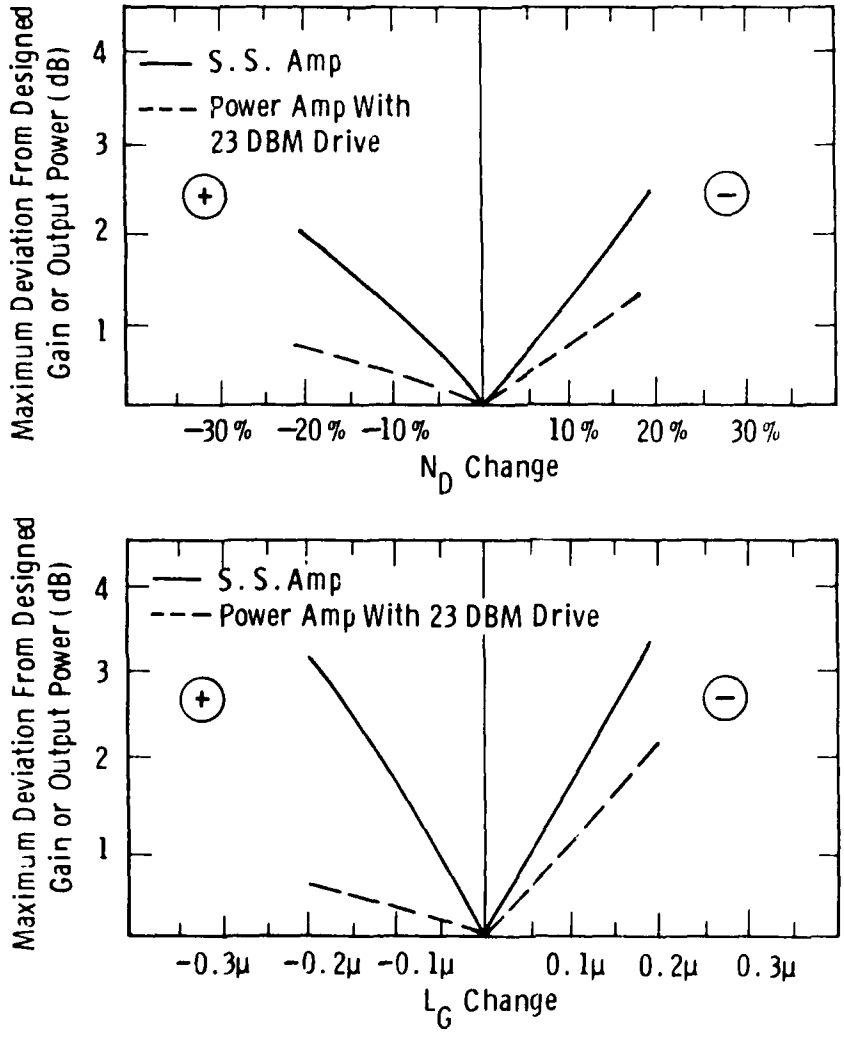
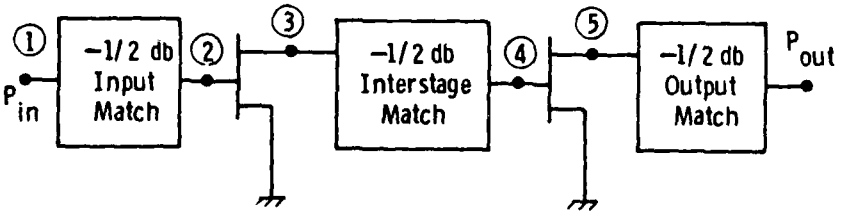


Figure 2-57. Maximum Gain and Output Power Change as a Function of Doping or Gate Length Variation for Two-Stage Small Signal Amplifier and Two-Stage Power Amplifier

output of the device and its small-signal lumped-element equivalent circuit is used for the input of the device. This simplifying assumption allows the power analysis to use COMPACT to determine load variations for each stage of the amplifier as a function of N_D and L_G variations in the active devices. Figure 2-58 shows a block diagram of this analysis for a two-stage amplifier.

The first step in the analysis is to calculate the load on the output of each transistor and the input mismatch to the first amplifier stage as a function of N_D and L_G using COMPACT. An input drive level to the amplifier is assumed (23 dBm in the case presented here); by substracting input reflection loss and matching circuit dissipative losses, the power level at the input of the first FET is determined. Since the drive level and load to the first FET have been uniquely determined, the load pull data yields the power gain from the first FET. Interstage loss is subtracted from this signal level, and the power level at the input of the output FET is determined. Again, the load contours and drive level determine the gain from the output FET. By subtracting the output matching circuit loss, the output power of the amplifier is obtained. Figure 2-57 illustrates the output power variation for



I. Calculate S_{11} @ ① to Determine Reflected Input Power Loss

II. Calculate S_{11} @ ③ & ⑤ to Determine Power Load to Input and Output FET

III. Assume an Input Signal and Calculate Drive Level at ②

IV. Use Load Contour Appropriate for Drive Level at ② and Determine $(P_{out})_③$ Using Load @ ③

V. Determine Drive Level @ ④ and Repeat Load Contour Plotting to Determine Final Amplifier Power

Figure 2-58. Large Signal MMIC Characterization Using Load Contours

the two-stage GaAs monolithic amplifier as a function of changes in L_G and N_D. The dashed curves of output power show less than 1-dB output power variation for a 10 percent change in either L_G or N_D.

Since the computation of gain (small signal) and power (large signal) variations in this amplifier showed the gain to be a sensitive indicator to the overall change in performance, the gain changes of amplifiers subjected to multiple process element variations have also been studied. In this case, all the process elements were varied simulataneously using Gaussian distributions. In all, seven process or device parameters were varied with the standard deviations shown below:

Parameter	Standard Deviation, %
N_D	10
L_G	10
Contact Resistance	30
Gate Metal Thickness	10
Output Resistance	10
Feedback Capacitance	10
Circuit Capacitors	10

An ensemble of 200 amplifiers was analyzed for nominal gate lengths of 0.9, 1.1, and 1.2 μm, which reflect wafer-to-wafer variation. The center value of the other variable distributions was not altered. As can be seen in figure 2-59, an RF yield of ~30 percent was obtained for an amplifier run whose nominal gate lengths was the 1.0-μm design value. The criterion used for acceptable performance was small signal gain within 1 dB of the original design value. As the average gate length on a wafer varied around the nominal 1-μm value, the yield of acceptable amplifiers dropped.

This RF yield approach will be used in the evaluation of possible circuit configurations for future monolithic power amplifier designs. The technique promises to provide information on:

(1) Design sensitivity to the expected standard deviation of process, device, and circuit parameters.

(2) Effect the shifts in the nominal or average value of a given parameter on the amplifier performance.

(3) Benefit of possible tighter control over the variation or standard deviation of any given process, device, or circuit parameter.

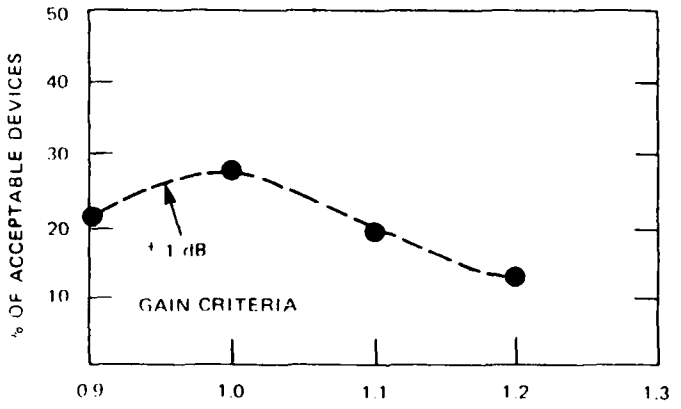


Figure 2-59. Statistical RF Yield of Two-Stage Amplifiers, Nominal Design vs Avg. Gate Length

Since any RF matching problem has a number of alternate solutions, it is possible to assess the manufacturability by searching for the least sensitive circuit which meets the original performance specifications. Acceptable goals can be established and confirmed on the computer before wafer processing begins.

3. 1 WATT 5-10 GHz TWO-STAGE AMPLIFIER

At the conclusion of Phase I, a two-stage, 5-10 GHz amplifier (Mark V) was still in processing. A 1200-μm first-stage FET was employed in the design, rather than the 900-μm FET used in previous designs, since it was determined that gain compression in the 900-μm FETs (resulting in low drive level for the second stage 2400-μm FETs) was responsible for not achieving the 1-W output power goal in those previous amplifiers. The gate lengths of the FETs were 1.0 μm. This amplifier is shown in figure 3-1. Note that air bridges (along with sparse vias) were fully integrated onto the chips at this time. In addition, both the air bridge and circuit metallizations (except the interdigital capacitors) were plated up to lower losses. Results of the amplifiers (Run IC20B) are shown in figures 3-2 and 3-3. The 1-W (30 dBm) output power level was achieved from approximately 5.5 to 8.5 GHz at an input power of 21 dBm (corresponding to 9 dB associated gain). Gain rolloff at the high end was attributed to long gate lengths due to problems with the FET masks. The power added efficiency of the complete, two-stage amplifier, however, was calculated at approximately 15.5 percent.

3.1 8-12 GHz TWO-STAGE AMPLIFIERS

A two-stage amplifier (Run IC31) using a 1200-μm first stage and 2400-μm second stage FET was designed and tested for the 8-12 GHz band. A new circuit mask was used in conjunction with the Phase I FET masks used for the Mark V amplifier. The FETs have 1.0-μm gate lengths. A schematic of the amplifier is shown in figure 3-4 and the small signal input and output matches are shown in figure 3-5.

Small signal gain ranged between 7.5 and 12.5 dB from 6.5 to 12 GHz (figure 3-6) with gain peaks at 6 and 12.5 GHz. The small signal gain peaks were attributed to approaching instability in the amplifiers. Power output, however, reached a maximum of only 27 dBm at 8 GHz, dropping down to 24 dBm at 12 GHz.

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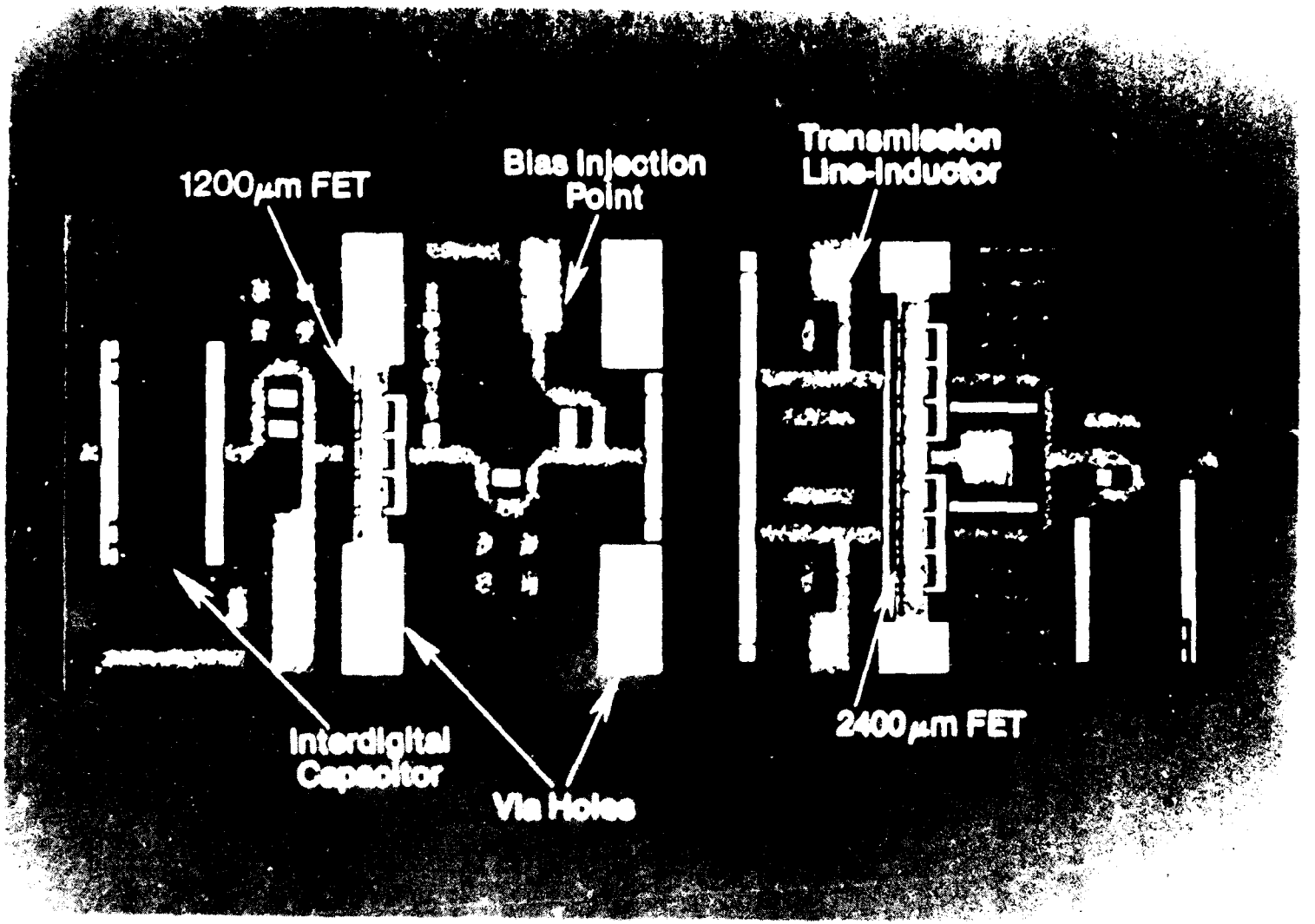

Figure 3-1. Two-Stage, 1-W, 5-10 GHz Amplifier (Mark V)

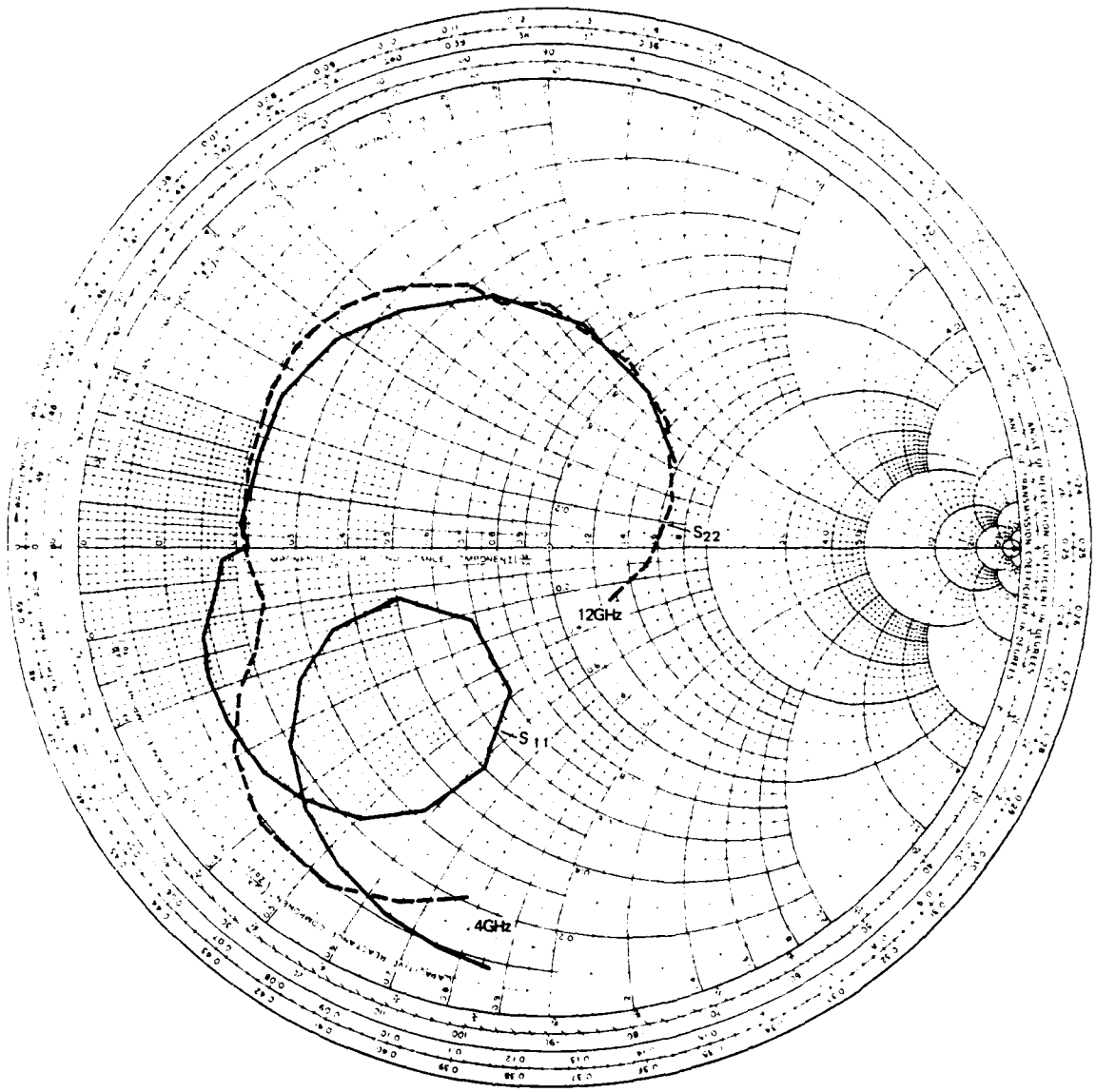

Figure 3-2. Mark V S_{11} and S_{22} Two-Stage Amplifier IC 20B12

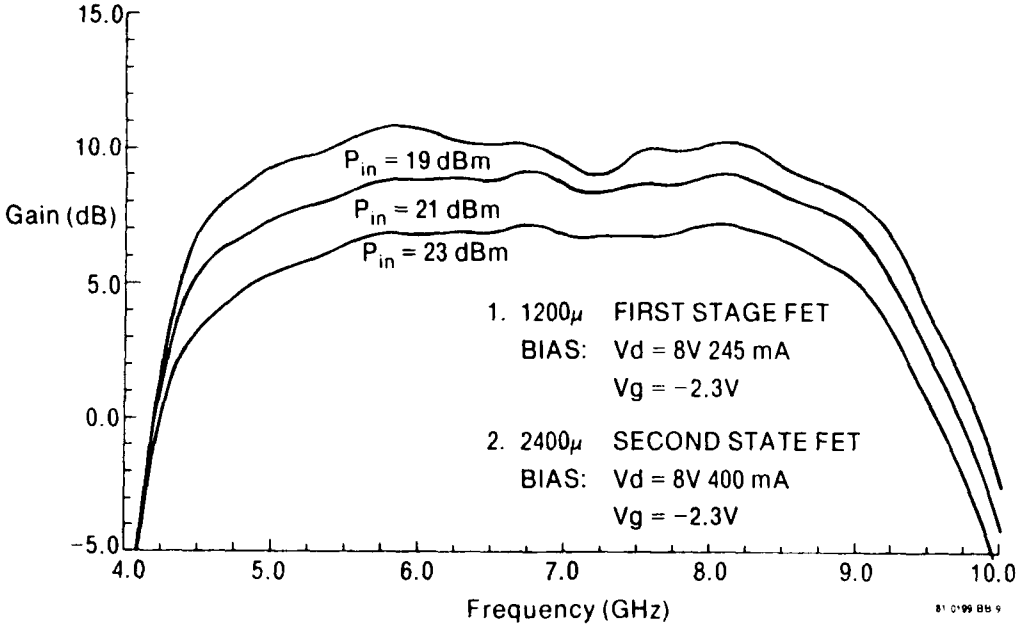

Figure 3-3. Two-Stage Monolithic Power Amplifier Gain (Mark V)

3.1.1 8-12 GHz, Two-Stage Amplifier with Overlay Capacitors

An 8-12 GHz, two-stage amplifier is currently in processing which incorporates several new fabrication and circuit design technologies. First, FETs with 0.7-μm gates formed by the deep UV photolithographic techniques described earlier are being used. Like the previous 8-12 GHz, two-stage design, a 1200-μm and a 2400-μm gate periphery FET are used for the first and second stages, respectively. Also, overlay capacitors are being used as tuning elements instead of the rather large interdigital capacitors used previously. Bypassing for bias will still be performed by off-chip hybrid capacitors.

A schematic of this amplifier (IC 40 and 42) is shown in figure 3-7. As usual, the 2400-μm output FET is divided into two 1200-μm FETs to improve source grounding (lower source inductance) and to alleviate the phasing problems associated with larger periphery FETs. However, a 25Ω isolation resistor has been added between the gates to reduce the possibility of oscillation between the two 1200-μm FETs. The 25Ω value was found to be optimal based on the calculated average isolation of the interstage circuit from 1 to 19 GHz. If the isolation scheme is implemented, a higher value

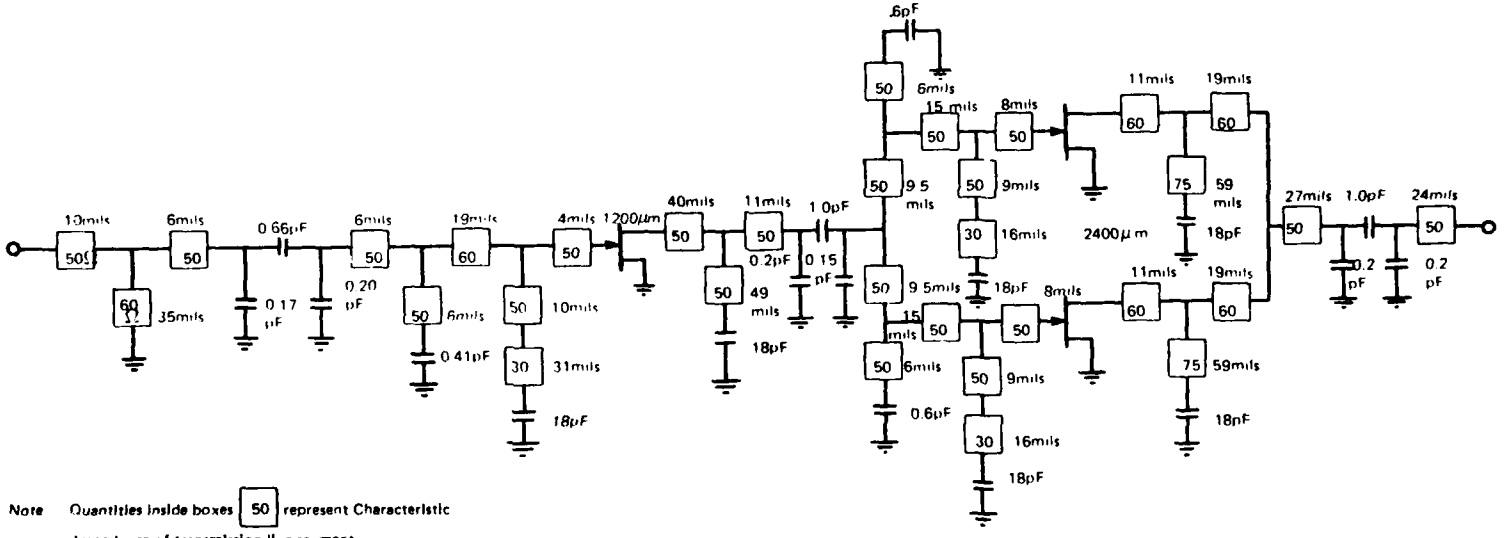

Figure 3-4. Mark VI Amplifier 8-12 GHz

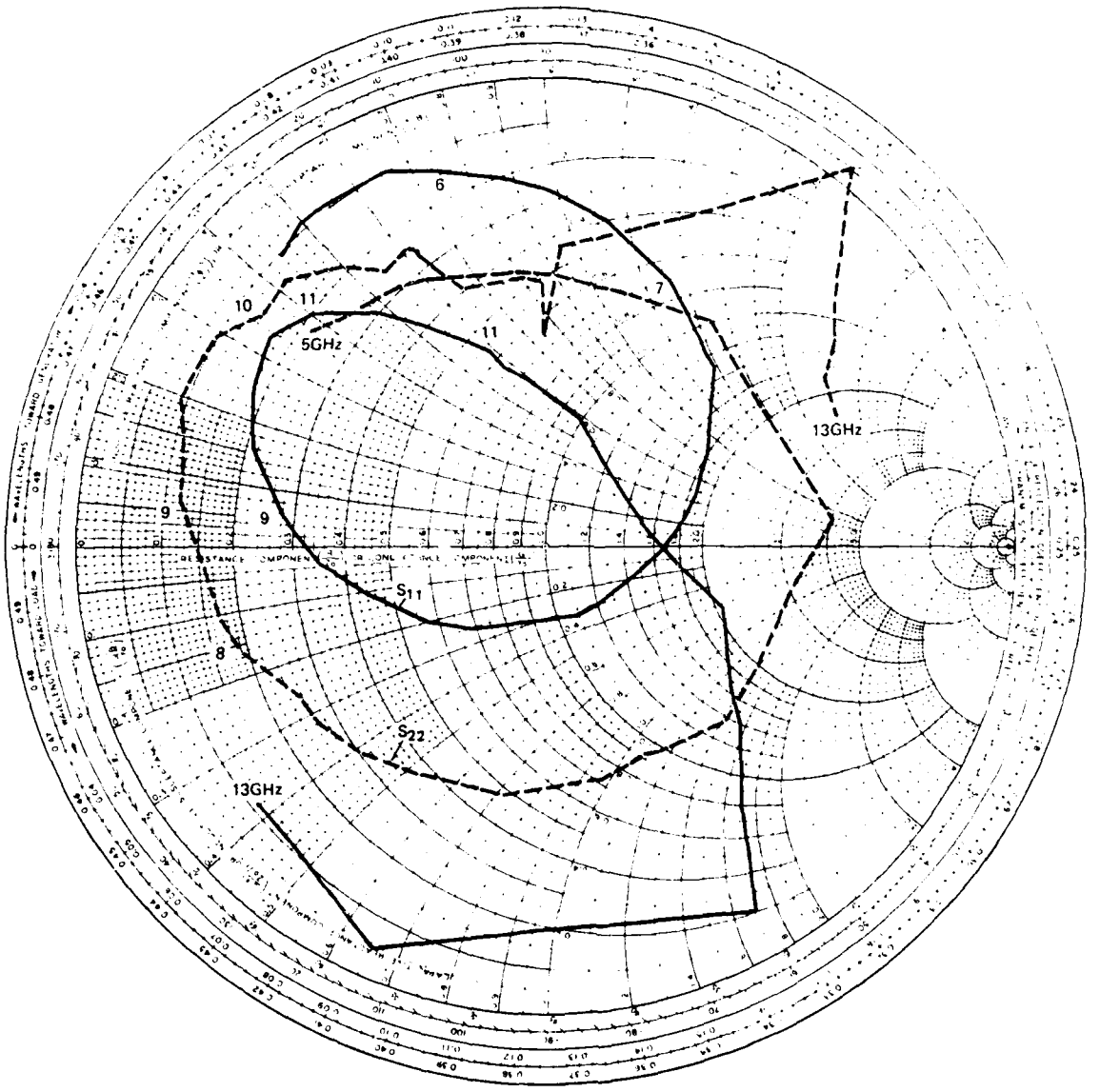

Figure 3-5. Two-Stage 8-12 GHz Amplifier S_{11} and S_{22}

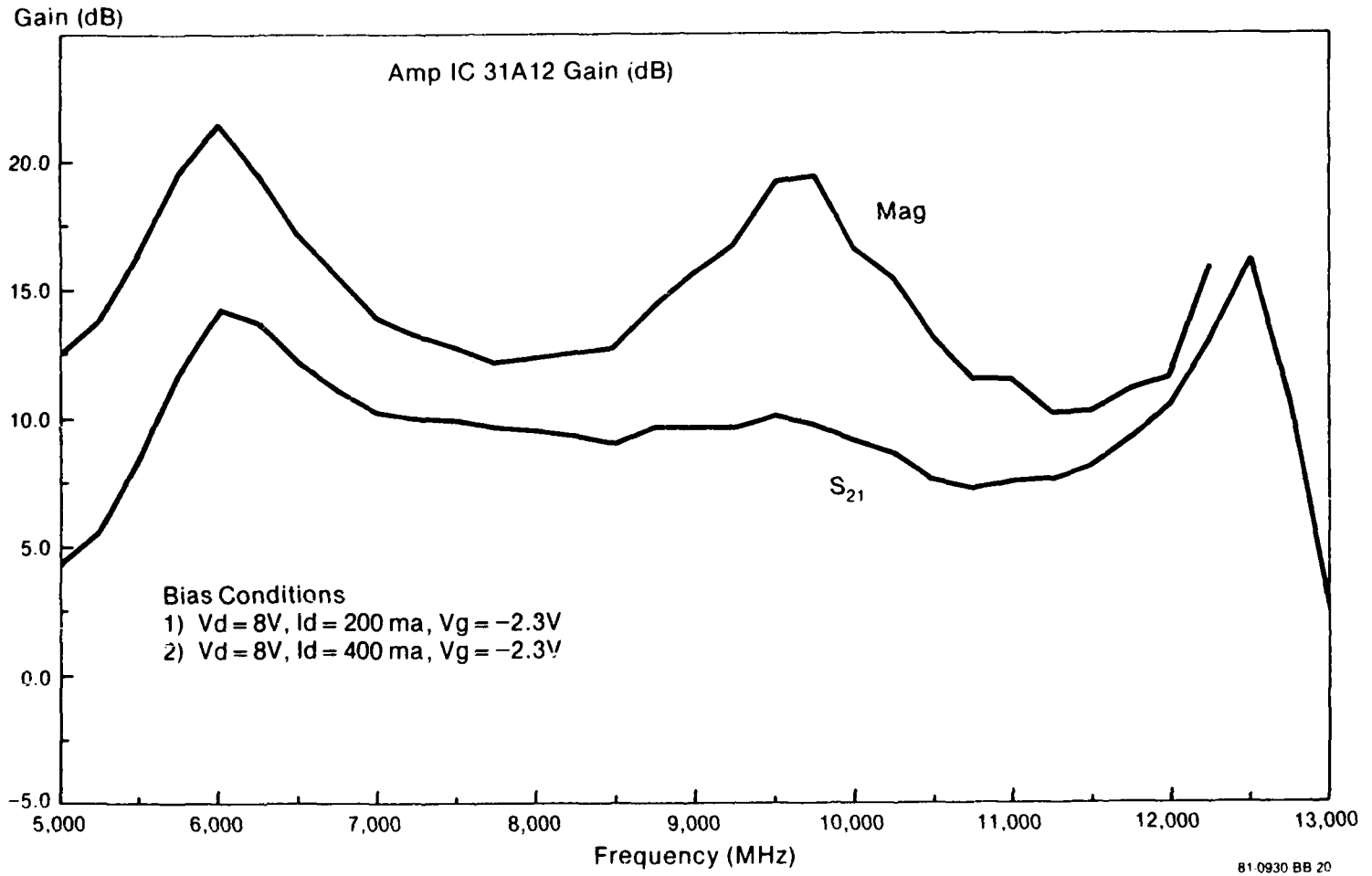

Figure 3-6. IC 31A4 Mark VI Amplifier Small Signal Gain (dB)

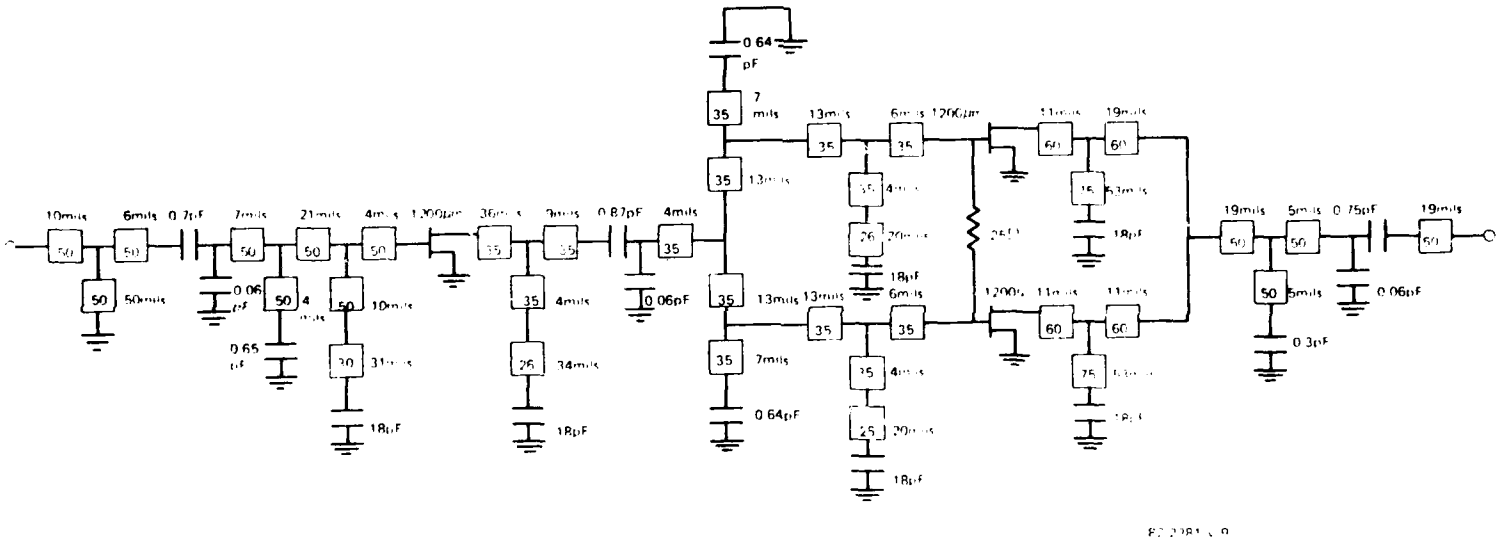

Figure 3-7. Two-Stage Amplifier (Mark VII Amplifier, 8-12 GHz) With Overlay Capacitors

resistor might be necessary due to the limited available range of the implanted resistors.

An improved interstage circuit was designed which presents an impedance locus to the first stage 1200-μm FET that curves inwards, at the upper band edge, towards 50Ω on the Smith chart instead of the usual outward direction (figure 3-8). A better high frequency power match is expected using this approach.

3.2 3-W, 8-12 GHz CLUSTER MATCHED AMPLIFIER

In order to achieve the 3-W output power goals for the four-stage Phase II amplifier, it is necessary to employ a large gate width ($\approx$ 6400 μm) FET in the final amplifier stage. Directly paralleling 32 200- μm cells, for example, in order to obtain the required 6400 μm total gate periphery results in an extremely low FET input impedance. Matching an impedance this low (1 to 2Ω) to 50Ω over a broad bandwidth is exceedingly difficult. More importantly, in a FET this large, phase differences between the cells close to the center feed point and those farthest away from the feed point cause a significant reduction in FET gain and power output. This is particularly true at X-band frequencies and above.

An alternative to direct cell combining through the use of a cell cluster matching design approach is shown in figure 3-9. In this approach, cells are grouped together into eight separate 800- μm cell clusters. The amplifier shown is the second iteration of a single-stage design which is power matched at both the input and output across the 8-12 GHz band (i.e., no gain slope compensation is used). The first iteration used four 1600- μm cell clusters. However, calculations indicated that the larger source inductance associated with a 1600- μm FET reduced its gain to an unacceptably low level. Note that the matching is done at the 800- μm cell cluster level where the input impedance levels are high. Each cell cluster is partially matching before combining, thereby resulting in an overall higher impedance level at the combining points and a corresponding improvement in performance over a broad bandwidth. Each cell cluster is first double tuned to a convenient resistive impedance level and combined with another partially matched cell cluster. A $\lambda/4$ transformer then transforms the combined resistive impedance level of each of the four cluster pairs to 200Ω . A convenient impedance level is defined as one which allows a practical line impedance to be used as the $\lambda/4$ transformer

1-19 GHz

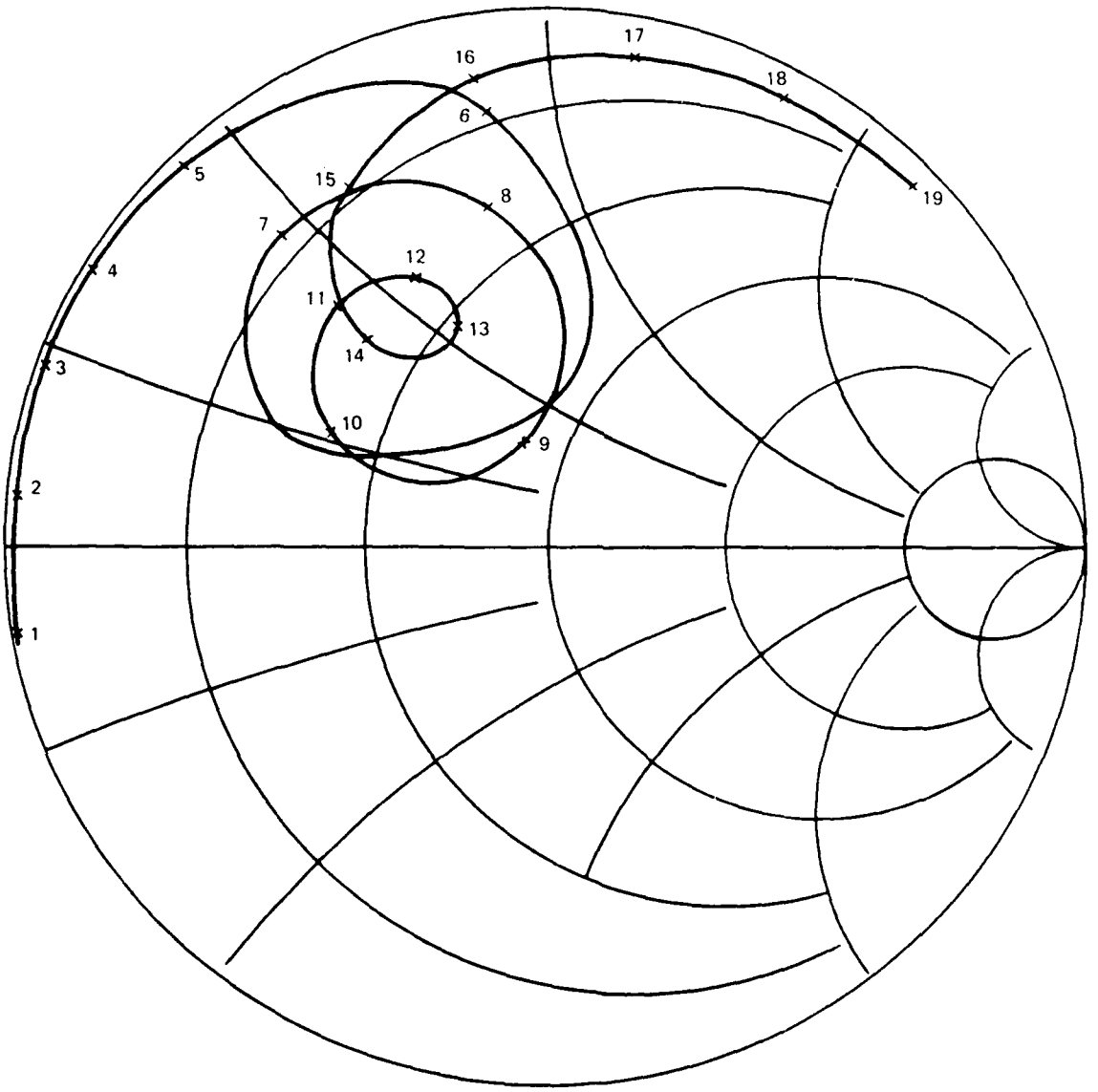

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Figure 3-8. Mark VII Interstage Locus, 1-19 GHz

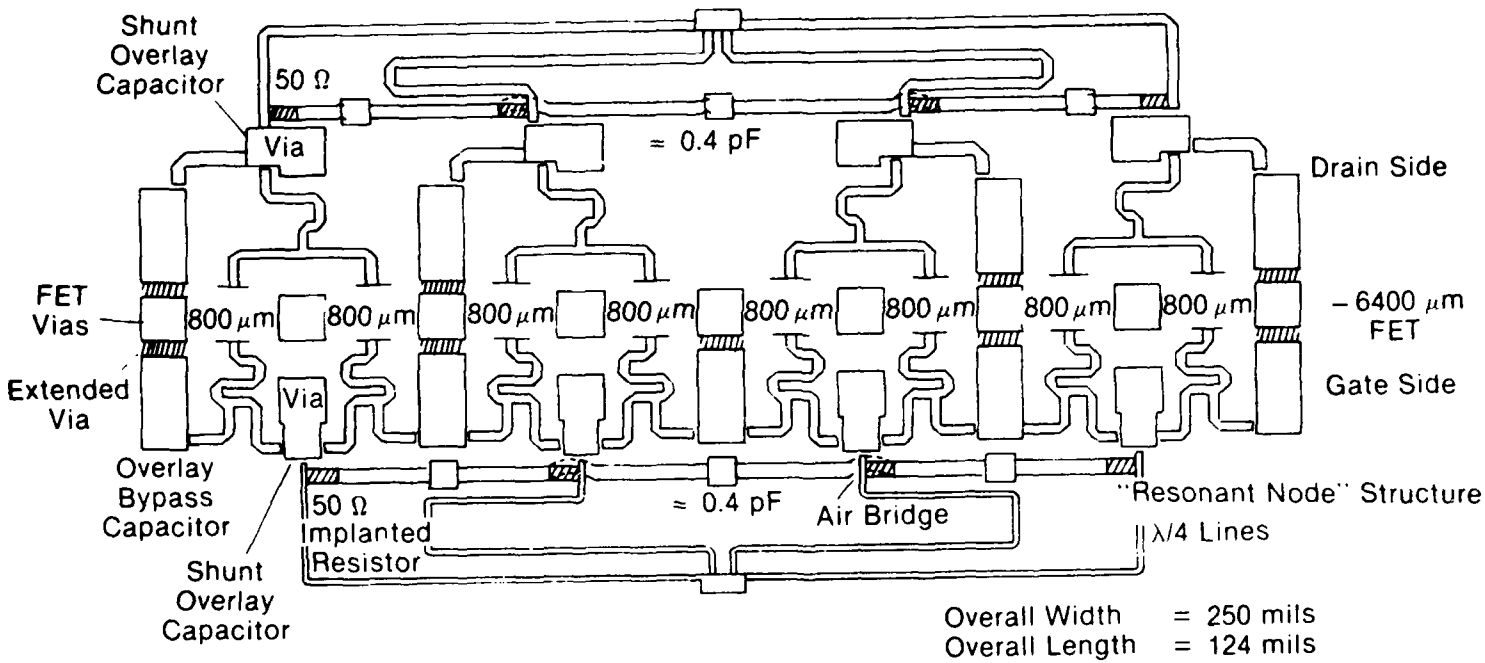

Figure 3-9. 3-W, 8-12 GHz Amplifier

while not severely complicating the initial double tuning circuitry. The four cell cluster pairs, now transformed to 200Ω , are combined to produce the desired 50Ω match.

Note that since the cell cluster matching circuits are identical, the phase angles of the wavefronts reaching each cluster are identical, thereby eliminating intercell phasing problems. Figure 3-10 shows an example of the impedance progression just described on the output or drain side of the single-stage, 3-W amplifier using four 1600- μm cell clusters. The intermediate impedance level in this design is 17Ω corresponding to 59 Ω λ/4 transformer. This 59-Ω value is obtained using the familiar equation

$$Z_o\ (\lambda/4) = \sqrt{Z_{o1} \cdot Z_{o2}} \quad \text{where } Z_{o1}$$

is the intial impedance level (17Ω) and Z_{o2} is the transformed impeda level (200Ω).

The calculated input and output power matches for this amplifier a. shown in figure 3-11. The small signal gain is shown in figure 3-12.

By placing resistors, whose values are equal to the resistive impedance level looking into each partially matched cell cluster pair, at the ends of each λ/4 line and tying the other end of each resistor to a common node, a four-way Wilkinson power combiner/splitter is formed. This type of combiner has good isolation characteristics over reasonably broad bandwidths. This isolation reduces cell-to-cell interactions and thereby minimizes amplifier performance degradation due to cell-to-cell variation. Unfortunately, on a planar structure, such as a monolithic amplifier, long inductive line lengths, and air bridges must be used to connect the isolation resistors to a common node. This inductance causes the isolation of the combiner to decrease with increasing frequency. To eliminate this effect, we have added series capacitors at the centers of each connecting line to resonate out the inductive effects at midband (10 GHz) and better approximate a short circuit. The calculated isolation characteristics of this "resonant node" structure are illustrated in figures 3-13 and 3-14 for the worst case (two outer ports) of the four-way input and output splitters. The isolation calculated is that seen by the FETs (i.e., FET capacitance and the initial matching circuitry are included). The implanted resistors used for isolation have a lower limit of

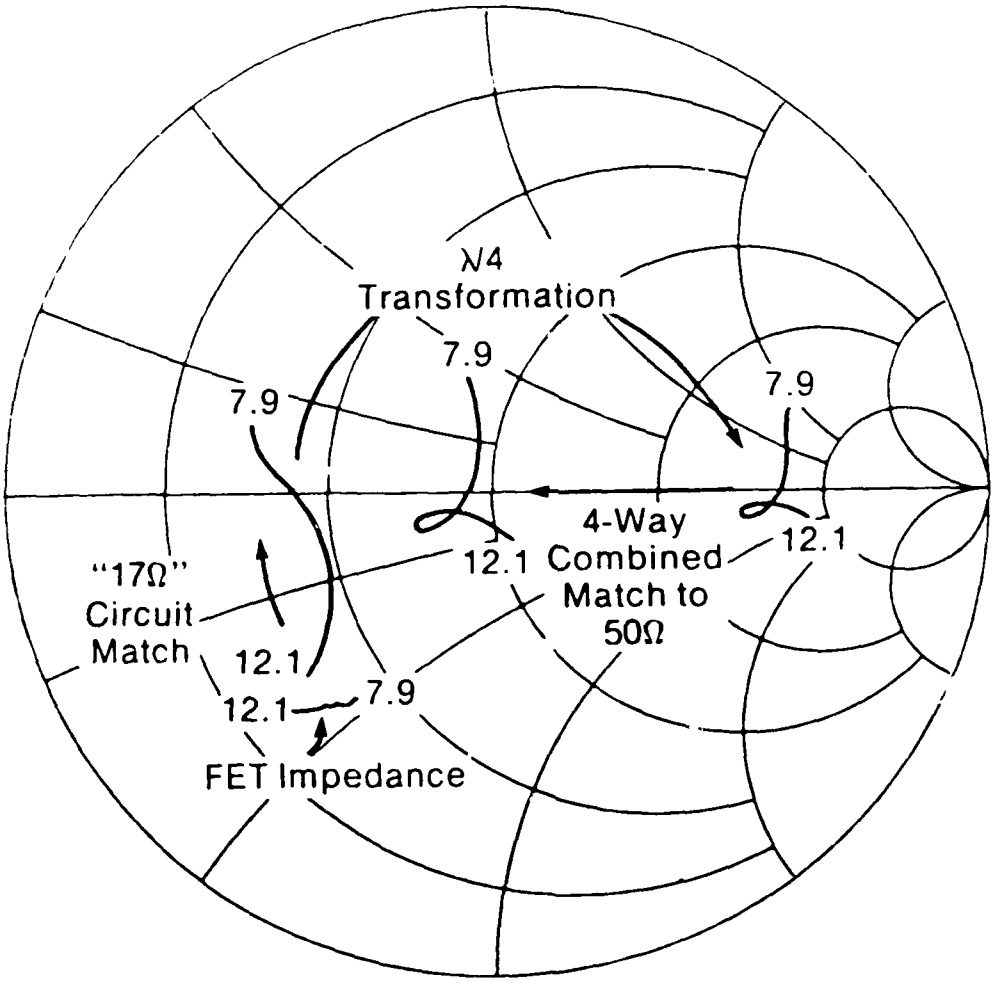

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Figure 3-10. Cell Cluster Matching

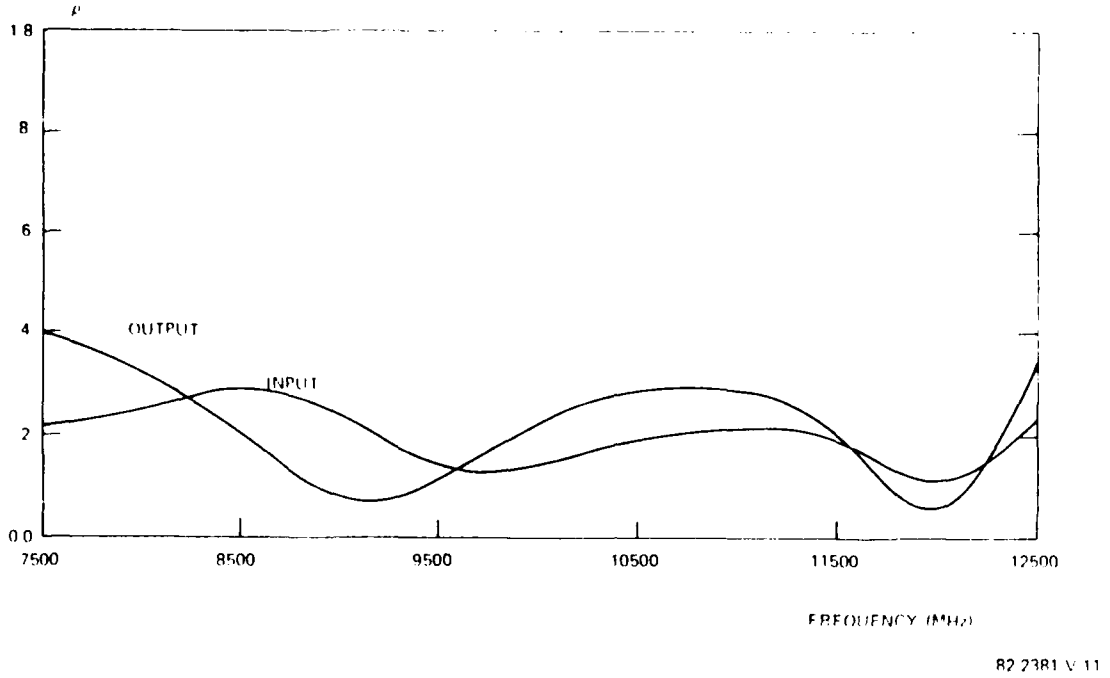

Figure 3-11. New 3-W Amplifier Power Matches

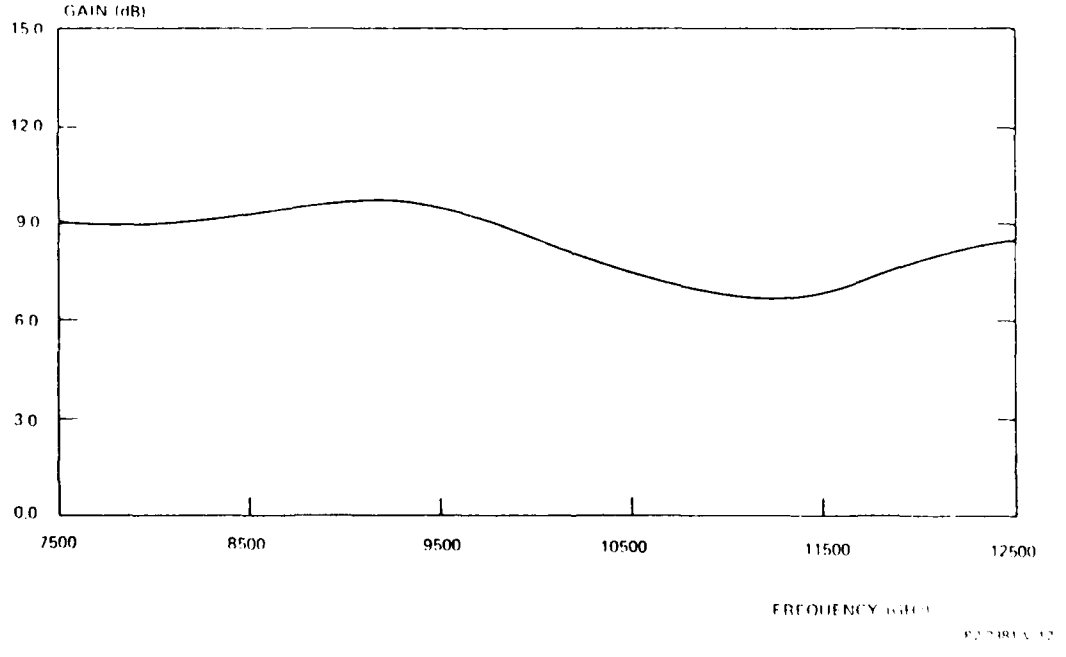

Figure 3-12. New 3-W Amplifier Small Signal Gain

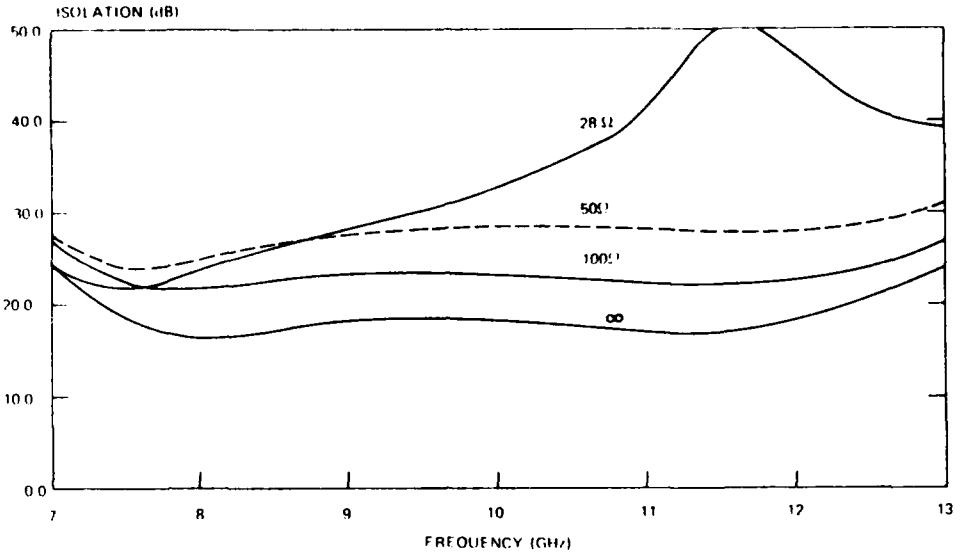

Figure 3-13. 3-W Amplifier Input Isolation vs Isolation Resistor Value

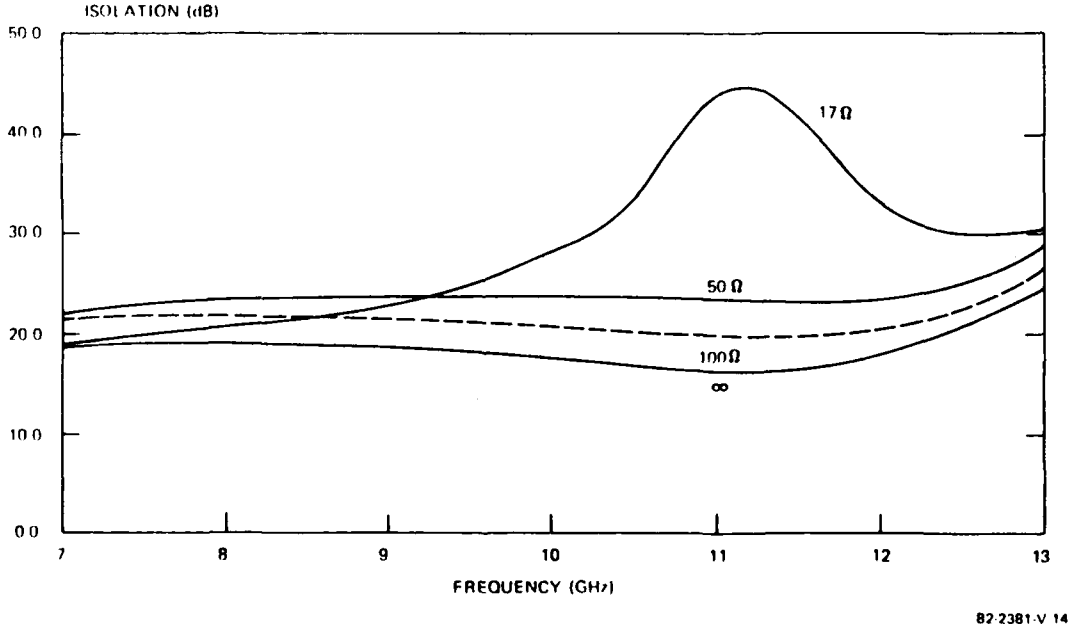

Figure 3-14. 3-W Amplifier Output Isolation vs Isolation Resistor Value

50Ω . A blowup of the input combiner section showing the implementation of the implanted resistors is shown in figure 3-15. Ideally, a 28Ω resistor should be used on the input splitter and isolations greater than 40 dB could be obtained. However, as can be seen by the curves in figure 3-13, isolation with 50Ω resistors is improved as much as 10 dB over the no isolation resistor case.

This amplifier was designed and laid out to determine where to place the implants for the 3-W output FETs. FET parameters (i.e., capacitances, resistances, g_m) were obtained by extrapolating Phase I FET (1.0 μm) parameters to the 800-μm gate periphery and the 0.7-μm gate length. FETs with 0.7-μm gates using both the parallel gate feed configuration and the new pi-gate configuration (D39) are being characterized at the conclusion of this reporting period. Redesign of the 3-W output stage is contingent upon obtaining consistent FET parameters from the discrete runs.

3.2.1 Four FET Hybrid Cluster Matched Amplifier

A four-FET hybrid (i.e., nonmonolithic) cluster matched amplifier was designed and tested in order to verify the basic cluster matching approach and resonant node isolation scheme that will be used in the 3-W, 8-12 GHz monolithic amplifier output stage. Small signal and high power FET characterization was performed on a large number of IC26 and 29 1200-μm (Phase I) devices. Since these FETs have 1.0-μm gates, the design band decided on was from 5 to 9 GHz. The 4-GHz bandwidth is equal to that for Phase II (8-12 GHz). In fact, the percentage bandwidth is higher for the hybrid study since the center frequency is lower. The IC26 and 29 1200-μm devices typically delivered between 400 to 500 mW from 5 to 9 GHz. Therefore, the four-FET amplifier was expected to deliver from 1.5 to 2 W in the design band.

A schematic of the first design iteration is shown in figure 3-16. The amplifier was designed to be power matched at both input and output across the 5-9 GHz band (i.e., no gain compensation). Two designs, one for IC26 devices and one for IC29 devices, were made. The IC29 design is shown in the figure. Duroid 5880 (Er = 2.2) was chosen as the carrier for the $\lambda/4$ splitter and combiner sections. The low dielectric constant substrate allows the $\lambda/4$ lines to be as long as possible in order to interconnect the fairly large hybrid circuitry. Each FET and its associated initial matching circuitry was placed

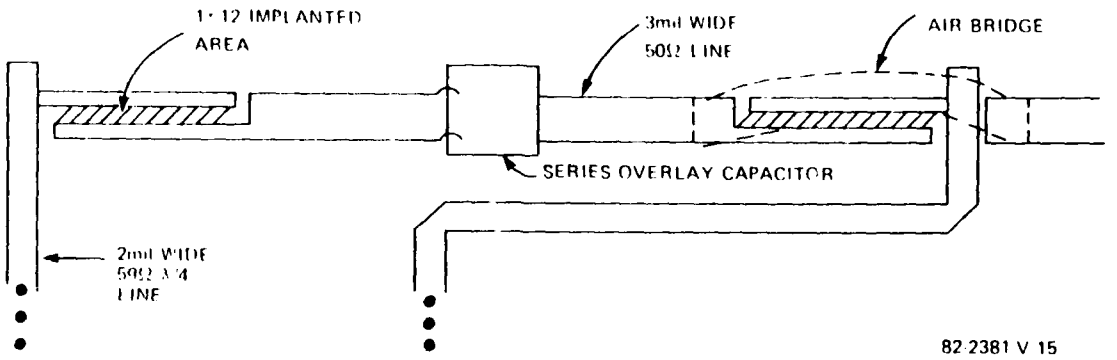

Figure 3-15. Blowup of Input (Gate) $\lambda/4$ Sections

on a gold-plated brass carrier which drops into the aluminum-backed Duroid piece. This approach allowed the FETs and their matching circuitry to be tested and tuned individually. The initial matching circuitry was placed on alumina pieces which were then placed on the brass carrier. Chip capacitors, bondwires, and transmission lines, etched on the alumina, were used as tuning elements. Via holes drilled through the alumina carriers and filled with gold provided grounding for the shunt tuning elements.

Initial testing of this design showed that the amplifier passband was too low (≈ 4 GHz). Subsequent studies indicated that the parasitic inductance associated with the via holes in the alumina carriers was too large, thereby shifting the passband down. The alumina carriers were then abandoned in favor of placing the tuning elements directly on the brass carrier.

The final amplifier single branch schematic is shown in figure 3-17. The resonant node isolation structure remained the same as in figure 3-16. The hybrid amplifier requires certain minimum bondwire lengths to interconnect its circuitry. Therefore, the input (gate) initial matching circuitry was slightly

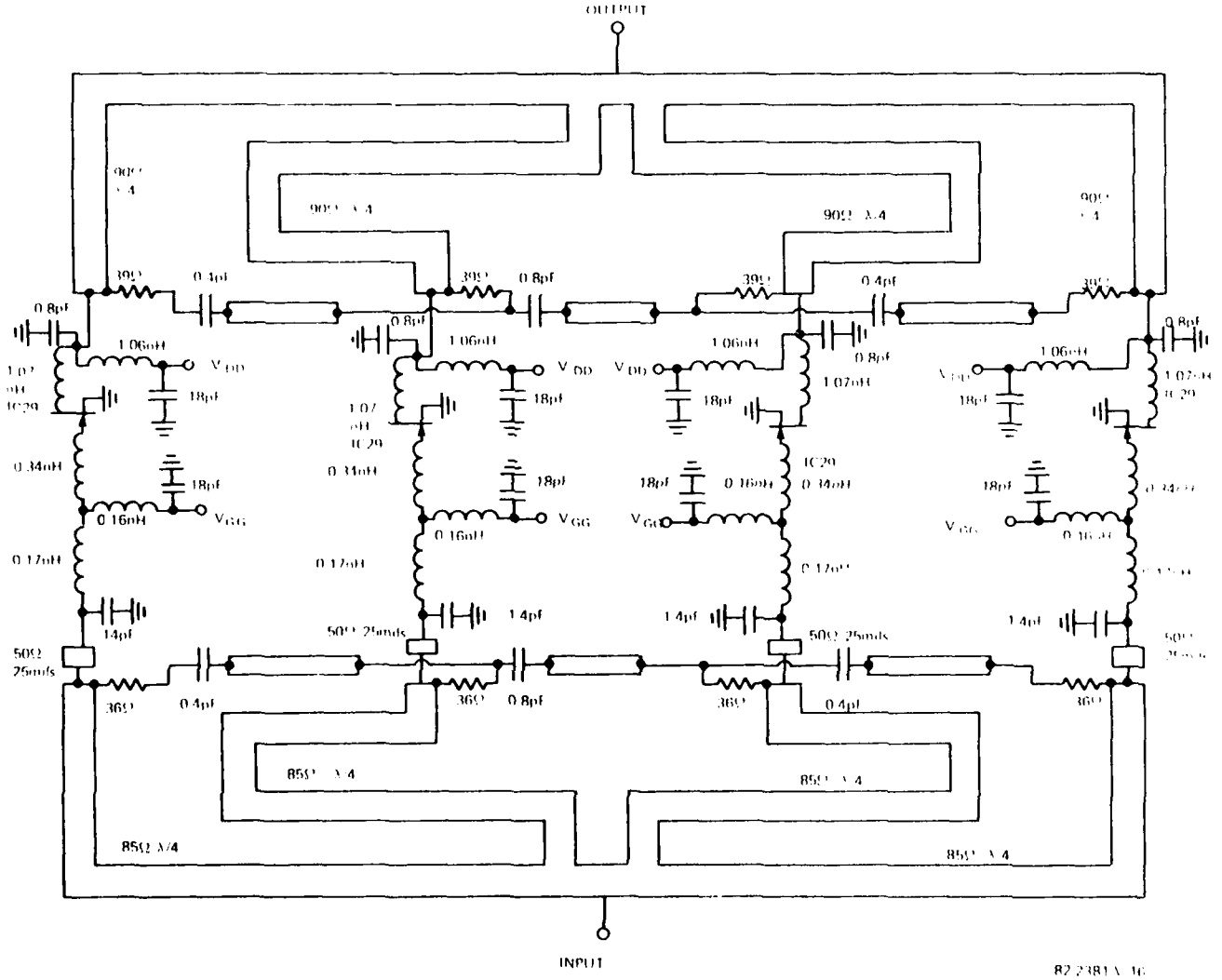

Figure 3-16. Hybrid Cluster Amplifier Schematic

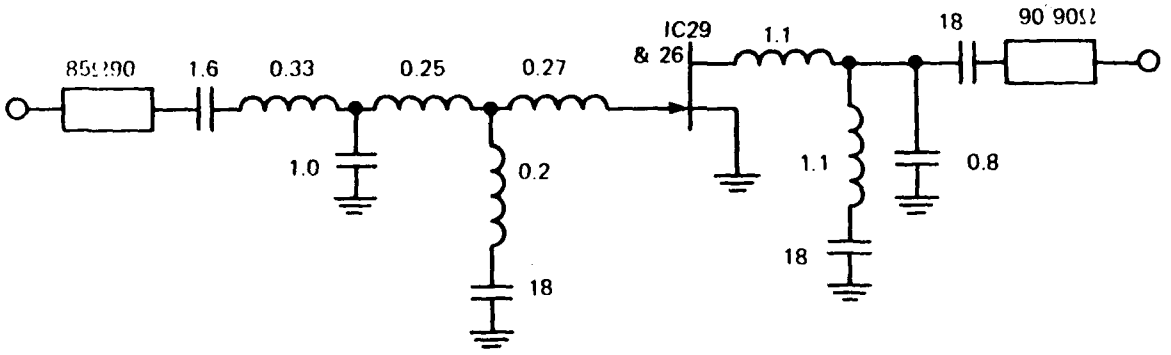

Figure 3-17. Hybrid Cluster-Matched Amplifier
Single Branch Schematic (Final)

redesigned to better absorb the extra inductance associated with these bond wires. The amplifier is shown in figure 3-18. Note that the FETs have independent biasing, thereby allowing each FET to run at its optimal bias point (particularly important for high power operation).

The small signal input and output matches are shown in figure 3-19. Computer backfitting of the input circuit model to the measured S_{11} indicated that the rolloff of the input match at high end of the band was due to a larger gate inductance than desired. The measured P_{out} vs frequency for various input drive levels is plotted in figure 3-20. 1.7 W was obtained at 6 GHz with 5.2-dB associated gain. The 3-dB bandwidth, however, only extended from 5.2 to 7.6 GHz. In addition to the input match problem described above and the inherent power rolloff of the FETs with frequency, phasing problems between the four branches of the amplifier appeared to be the main reason for lack of bandwidth. The phase deviations from port to port for the FETs and their initial matching circuitry are shown in figure 3-21 and for the $\lambda/4$ combiner sections in figure 3-22. The phase deviations are referenced from port 1. As can be seen, the phase differences between the four branches are

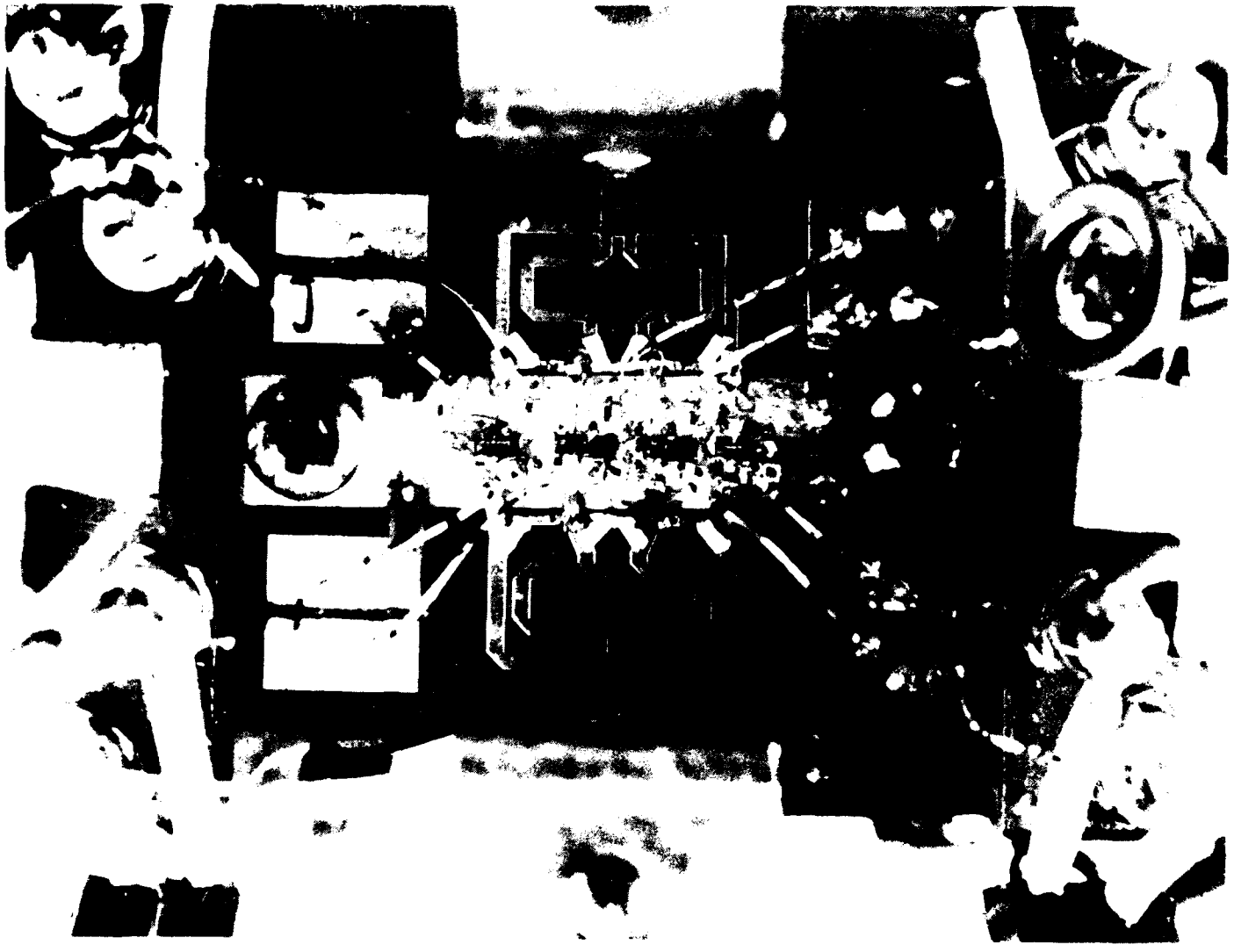

Figure 3-18. Four-FET Hybrid Cluster Matched Amplifier

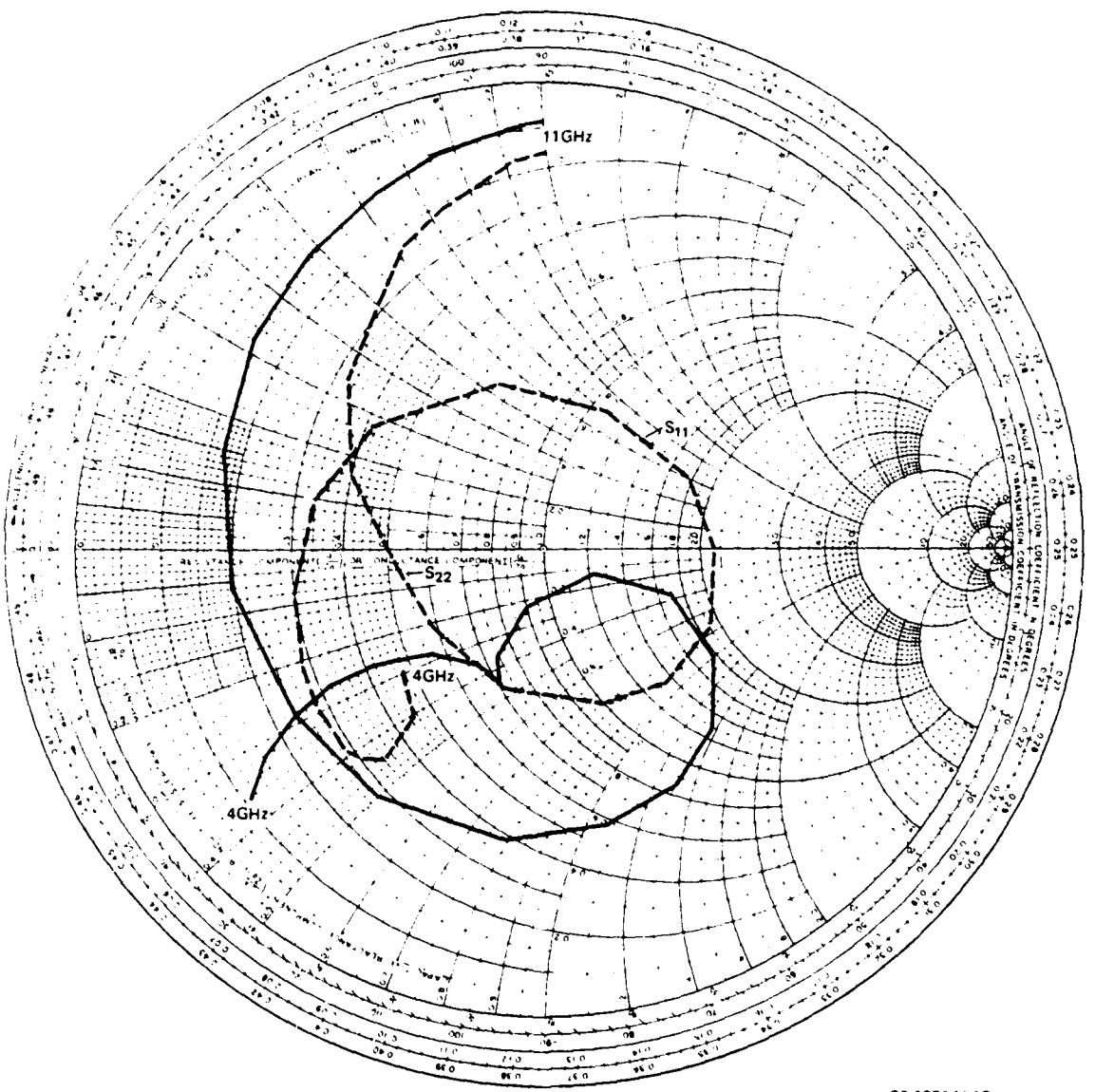

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Figure 3-19. Hybrid Amplifier S_{11} and S_{22}

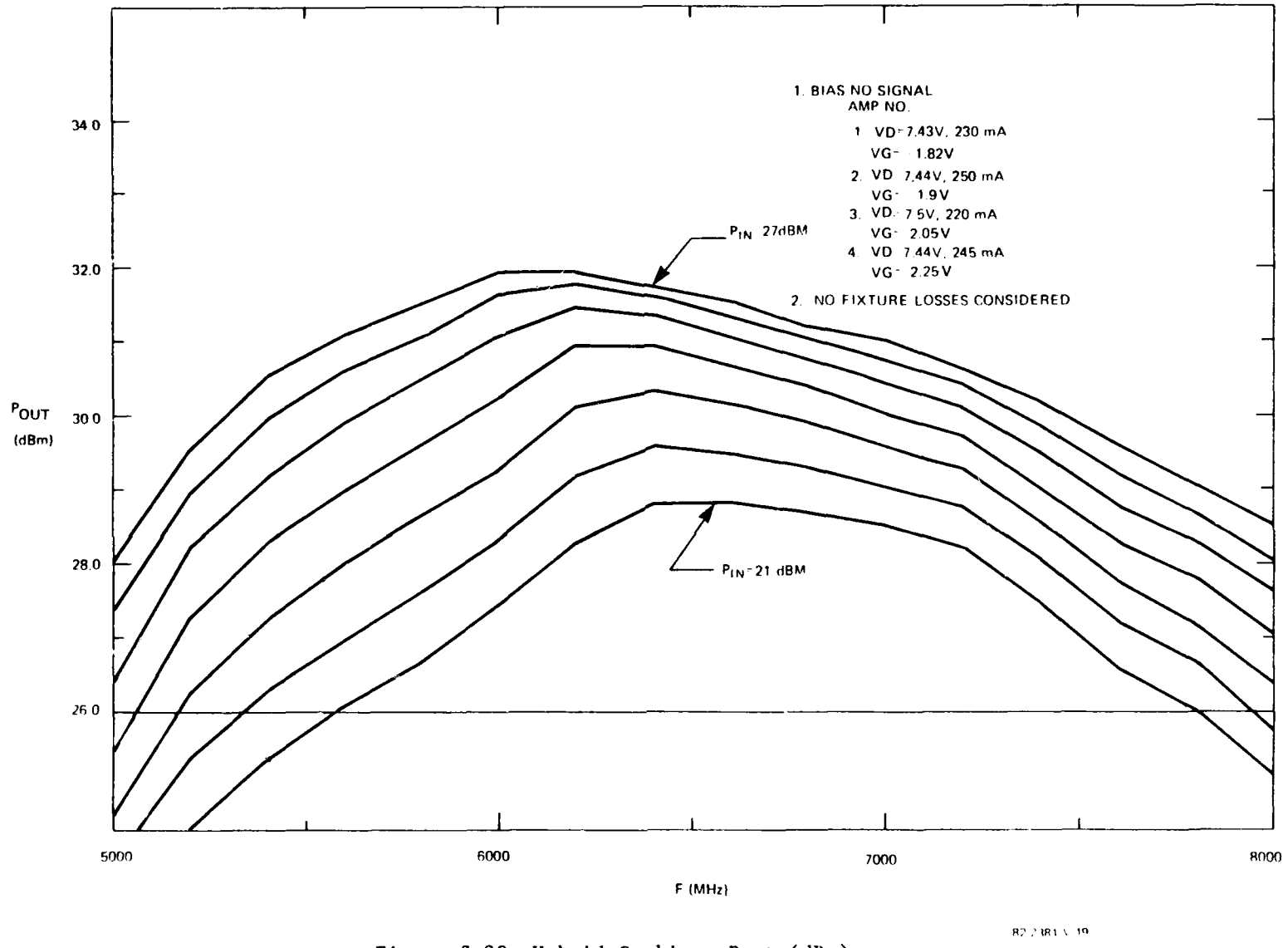

Figure 3-20. Hybrid Combiner Pout (dBm)

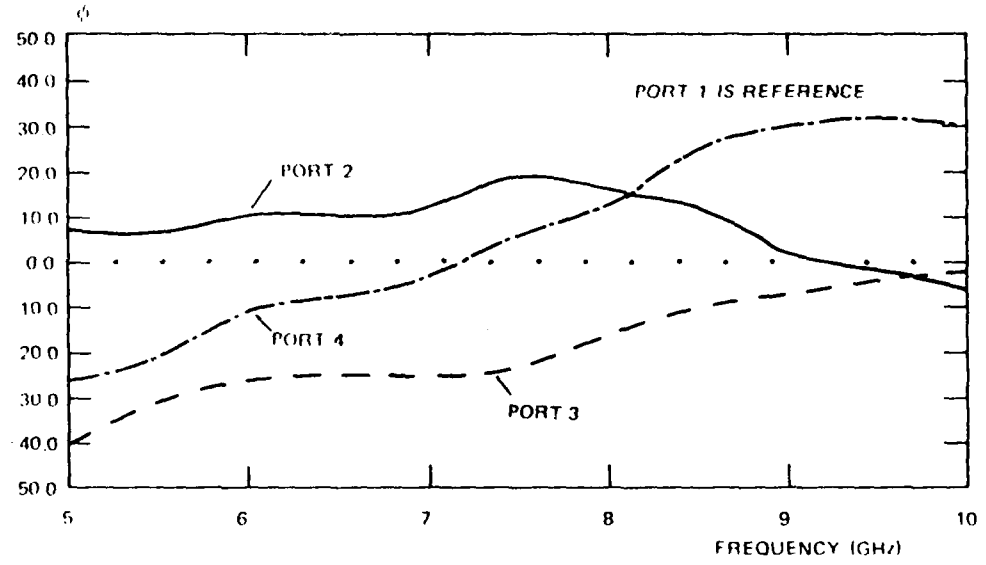

Figure 3-21. Hybrid Cell Cluster S_{21} Phase Deviation

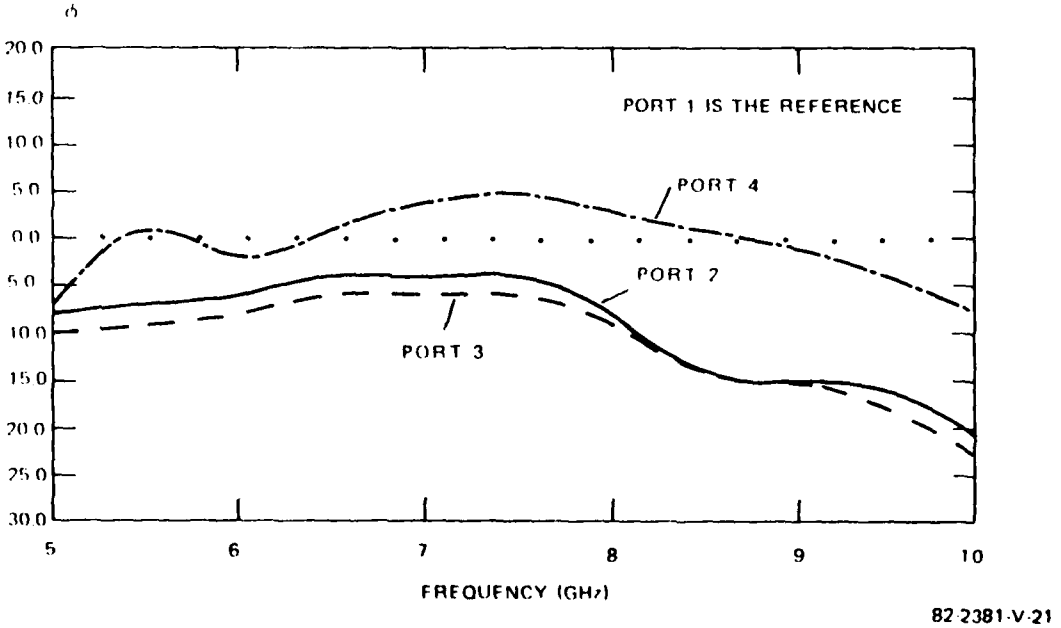

Figure 3-22. Hybrid Combiner Port-to-Port Phase Deviation

significant causing combining efficiency to drop along with power output and gain. These phase differences were attributed to the fact that FETs from various runs and wafers were used in addition to slight variations in the individual matching circuits. Neither one of these problems should appear in a monolithic implementation of the cluster matching approach (see figure 3-23: Monolithic "Cures" for the Inherent Design Problems of the Hybrid Cluster Matched Amplifier).

Figure 3-24 shows the improvement in isolation between the worst case ports (two outer) using the resonant node isolation structure. The isolation improvement averaged 10 dB from 5 to 10 GHz over the with isolation resistors - no resonant node case and even higher over the no isolation resistor case. Peak isolation for these ports was over 30 dB, approaching 50 dB between other ports.

3.3 FIRST-STAGE AMPLIFIER STUDIES

The design approaches to stages two, three, and four of the four-stage Phase II amplifier are basically fixed at this time. Stages two and three are being designed, as stated earlier, in the same manner as the two-stage Phase I amplifiers. Also, the cluster-matching approach was developed for use in the 3-W final stage containing the large 6400-μm gate periphery FET. However, in the first (low power) stage, several design approaches are being considered. In addition to the conventional approach being used in stages two and three, feedback and active matching techniques are being studied. Three first-stage designs were made, each using one of these design approaches. The fact that the first stage is low power allows the use of the feedback and active matching techniques, since power output and power-added efficiency of the overall amplifier are not significantly affected.

The conventional amplifier design is shown in figure 3-25. In the conventional design approach, the full burden of gain equalization for each FET is placed on the circuitry immediately following that FET. Therefore, the input is flatly matched across the 8-12 GHz design band.

The feedback amplifier design is shown in figure 3-26. A drain-to-gate (voltage sample-current sum) feedback network is used. The feedback network improves the input and output match of the 600- μm FET, thereby allowing simpler input and interstage circuits to be used. Unfortunately, the price paid for this simplicity is lower first-stage gain.

1. Smaller size allows easier layout of combining circuitry; branch-to -branch coupling is reduced

2. Identical matching circuits and FETs for equal phasing across a broad bandwidth

3. Lower parasitics (low inductance vias)

4. Microstrip has more predictable characteristics (vs using a bond wire)

5. Shorter line lengths can be used, thereby preserving bandwidth

6. Inherent monolithic advantage of placing matching circuitry close to the FET.

Figure 3-23. Monolithic Cures for the Inherent Design Problems of the Hybrid Cluster-Matched Amplifier

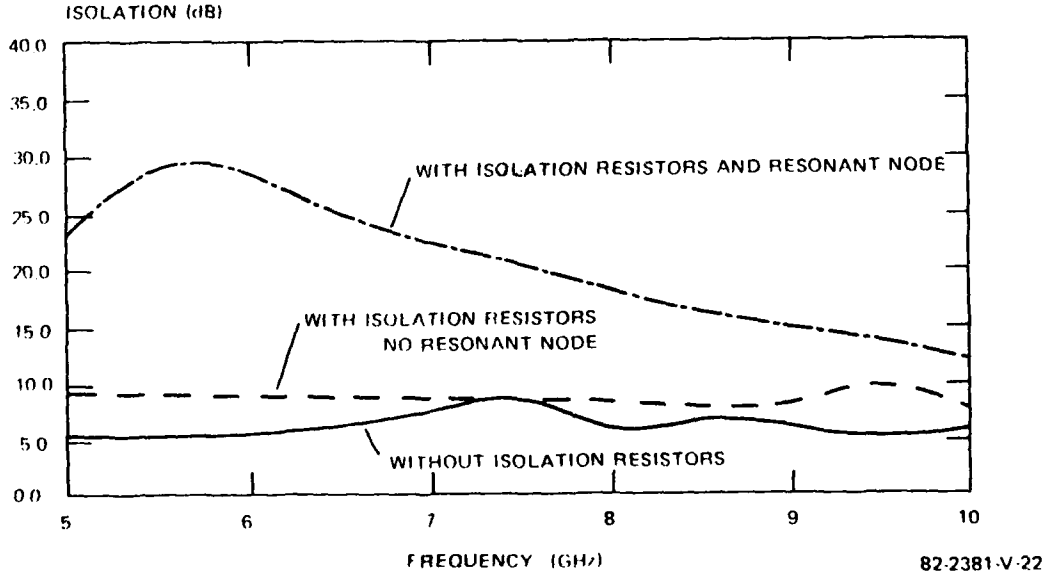

Figure 3-24. Hybrid Combiner Port 1 to 4 Isolations

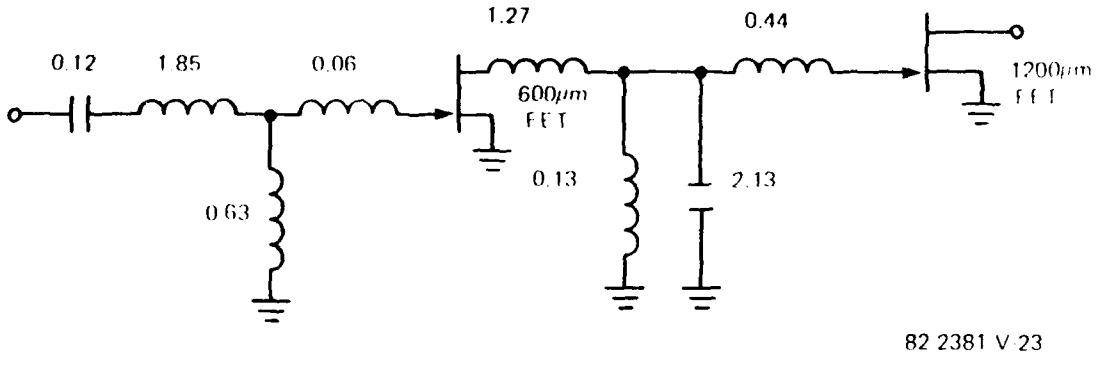

Figure 3-25. Conventional Amplifier Design

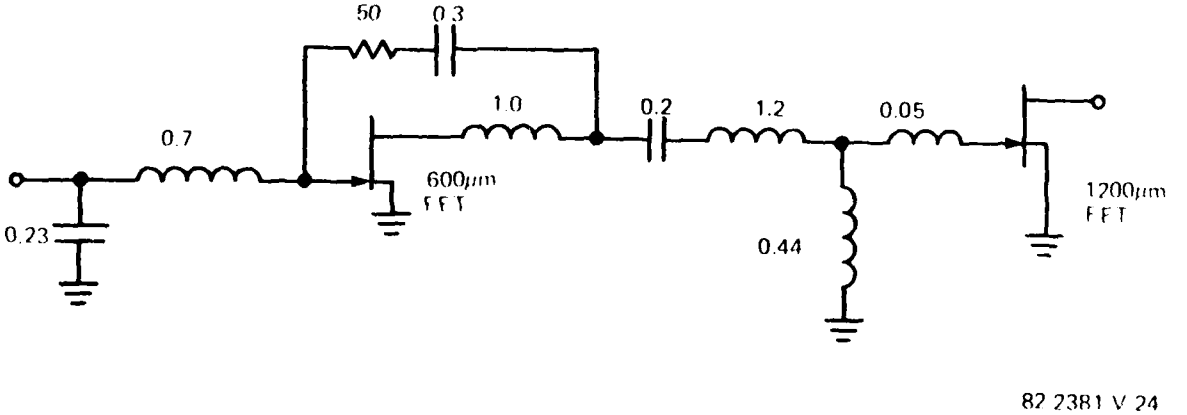

Figure 3-26. Feedback Amplifier Design

Some basic principles of active matching are shown in figure 3-27. The common gate FET configuration has an input impedance approximately equal to $1/g_m$. This approximation is very good at low frequencies, but becomes less valid at the higher microwave frequencies (above 5 GHz) due to FET capacitances. Therefore, for a 50-Ω match, a g_m of 1/50 or 20 mv is required. This g_m value corresponds to a gate periphery of about 300 μm. Similarly, the common drain or source follower configuration has an approximate output impedance of $1/g_m$. A gate-to-source feedback resistor is sometimes included, in this configuration, to form an active impedance transformer. A schematic of the amplifier designed using active matching is given in figure 3-28. To stabilize the common gate FETs, neutralizing inductors were required. Typical common gate designs used for matching do not require these inductors. It is believed that the use of extrapolated FET models instead of actual measured FET parameters for the 0.7- μm devices is the reason for the need to include these inductors. As a result, calculations indicated that a 600- μm common gate FET provided a better input match than a 300- μm device. Since the common gate configuration has unity current gain, a high impedance load must be applied to it to obtain voltage (and power) gain.

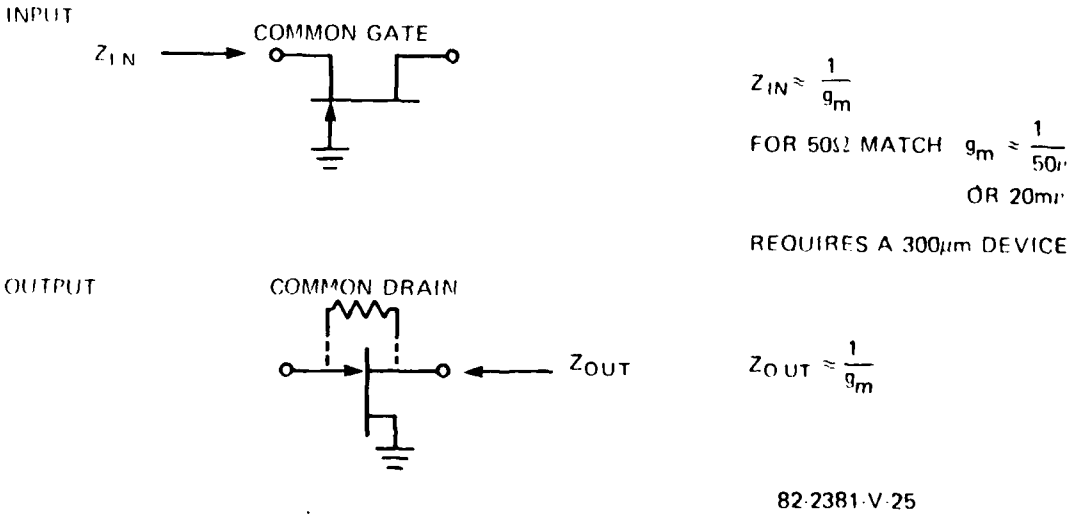

Figure 3-27. Active Matching

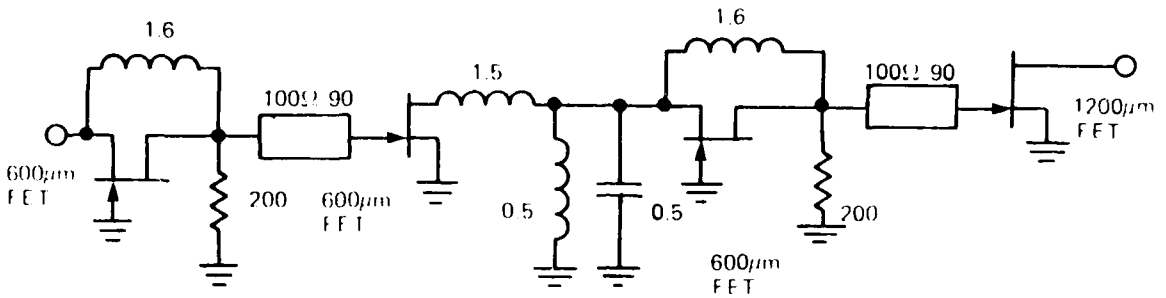

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Figure 3-28. Actively Matched Amplifier Design

The $\lambda/4$ transmission lines transform up the low common source input impedance of the following FET for this purpose. The 200Ω resistors provide both gain equalization and FET stabilization functions.

A comparison of input match and gain for the three designs is given in figures 3-29 and 3-30, respectively. As expected, the best input match is obtained from the feedback and actively matched designs. The feedback design, however, does suffer from low stage gain. A comparison chart of the three designs is shown in figure 3-31. The three were compared on the basis of input match, gain, total gate periphery required, total circuit inductance, total circuit capacitance and gain sensitivity to a $\pm$20% change in doping density (corresponding to a $\pm$10% change in gate-to-source and drain-to-source capacitances). Note that the actively matched amplifier, as designed, requires 1200 μm of extra gate periphery. This not only impacts power added efficiency, but complicates the amplifier biasing. The feedback amplifier, with its good input match, simple circuitry, and low sensitivity to FET variation, appears to be the best choice for the first stage at this time.

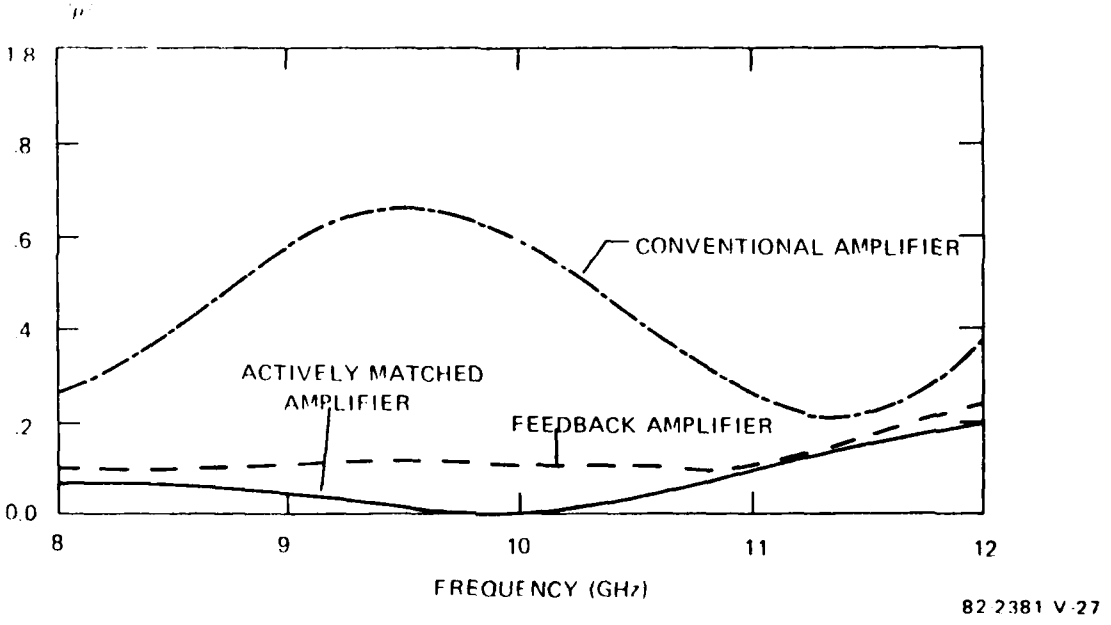

Figure 3-29. Input Match Comparison

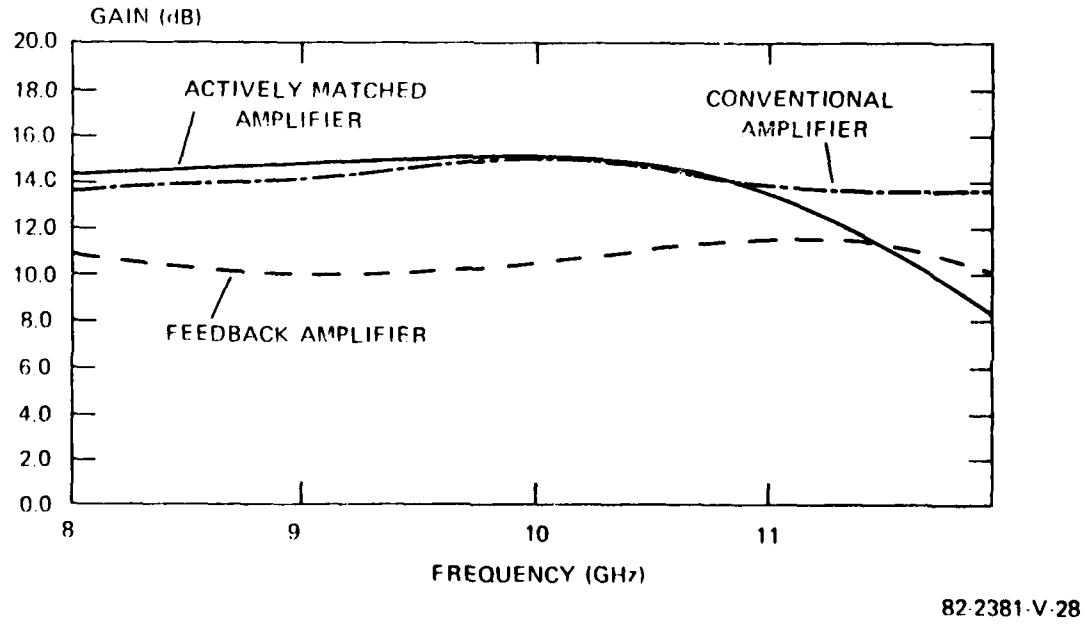

Figure 3-30. Gain Comparison

	CONVENTIONAL AMPLIFIER	FEEDBACK AMPLIFIER	ACTIVELY MATCHED AMPLIFIER
INPUT MATCH	POOR (8dB R.L.)	VERY GOOD (20dB R.L.)	EXCELLENT (26dB R.L.)
GAIN (dB)	14.5	10.5	14.5
TOTAL GATE PERIPHERY (μm)	1800	1800	3000
TOTAL (pH) INDUCTANCE	4.4	3.4	2.0 pHs 2.3/4 x Lmin
TOTAL (pF) CAPACITANCE	2.25	73	5
AVG. GAIN VARIATION FOR ±20% DOPING DENSITY CHANGE	-2.1 TO 1.6	-1.2 TO 1.0	-2.0 TO 1.6
OTHER		50Ω FEEDBACK RESISTOR	TWO 200Ω RESISTORS

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Figure 3-31. Comparison of Three Amplifier Design Approaches

4. REFERENCES

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(5) R.A. Pucel and C.F. Krumm, "Simple method of measuring drift-mobility profiles in thin semiconductor films," Electron. Lett., vol. 12, p. 240, 1976.

(6) BMDP, Biomedical Computer Programs, P Series 1979, University of California, Los Angeles.

(7) The Large Signal element values of the FET as a function of drive level are replaced by using the load pull contours representing the effect of output loading on the large signal performance of the device.

(C1) Solid State Scientific, Montgomeryville Industrial Park, Montgomeryville, Pa. 18936.

(C2) Micro Mask, 695 Vaqueros Ave, Sunnyvale, Ca. 94086.

(D1) J.E. Davey, Private Communication.

APPENDIX A

INSTALLATION OF ALLOYING FURNACE

The fabrication of devices on full 3-in. diameter wafers requires an alloying furnace capable of producing uniform heating of the wafer to carefully controlled temperatures for short periods of time.

The furnace used in this study is a Lindberg Lancer diffusion furnace with twin 5-in. diameter process areas. Each process area is divided into three individually controllable temperature zones where the temperature of the center zone is set at 620°C in this alloying process. The temperature profiles of the furnace have been measured under various combinations of temperature settings. The best profile is shown in figure A-1 where the deviation of temperature within the 20-in. flat center zone is less than $\pm 5^{\circ}C$.

The quartz process tube has an outside diameter of 120 mm and is 84 inches long. It is inserted into the furnace with the capped end extending 20 inches outside the furnace. Inside the tube, a triangular-shaped rack is laid with one end against the rear end of the tube. It ensures the graphite boat sits in the same alloying temperature zone each time the boat is pushed into the furnace. A quartz parallel-bar rail is put inside the tube with one end against the stopper rack and the other end extending the copper-end of the process tube. It serves as a supporting and guiding rail for the boat to slide easily in and out. Figure A-2 shows the arrangements of the furnace and the process tube.

The process boat is made of high density graphite, 4.5 in. long by 3.5 in. wide by 1/2 in. thick, and its position in the tube is controlled by a 5-ft. long, small diameter quartz tube attached to a point under the boat. A chromel-alumel thermocouple wire is embedded in the boat to monitor its temperature, which is displayed on an Omega digital thermometer and recorded vs time by an Esterline recorder. A typical temperature profile for the alloying cycle is shown in figure A-3.

The forming gas used in this alloying furnace is a mixture of 10 percent hydrogen and 90 percent argon flowing at a rate of 4.5 ft^3/hr, which provides one tube volume of gas every 10 minutes. The tube is continually flushed with nitrogen when the furnace is not used for alloying. The carbon boat is more massive than previous designs to improve the uniformity of heating and this reduces the rate at which the boat cools. To restore the fast rate of cooling required for successful alloying, the boat is cooled by

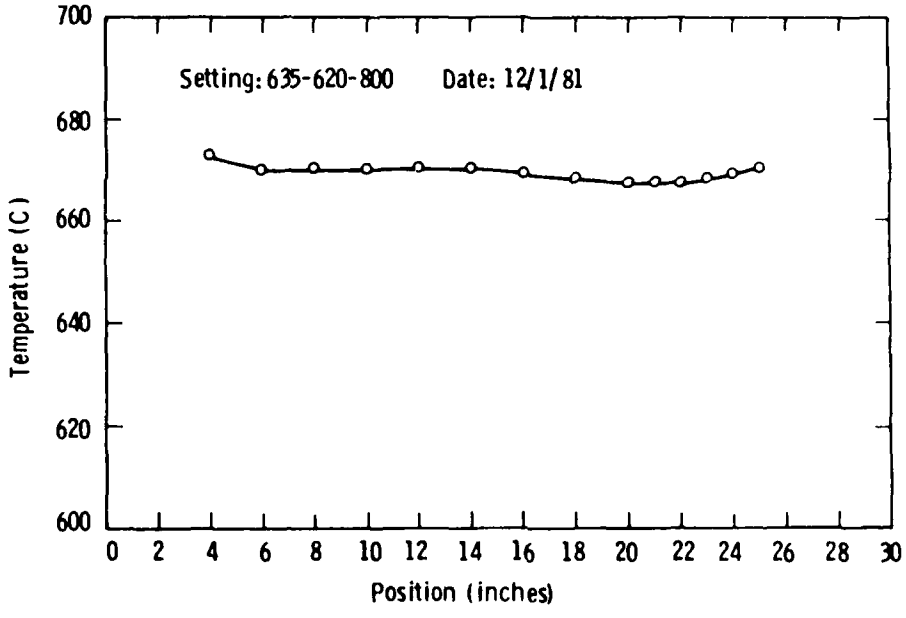

Figure A-1. Alloy Furnace Temperature Profile

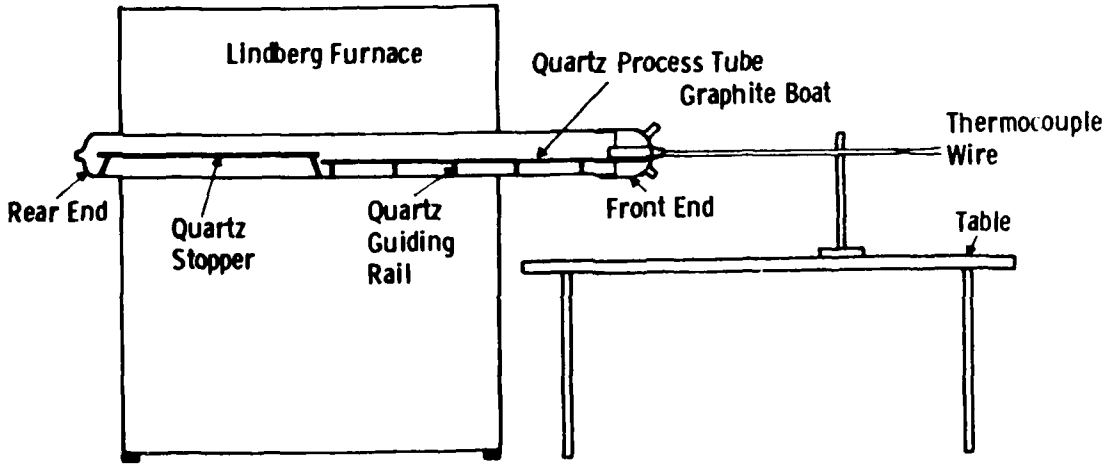

Figure A-2. Alloy Furnace and Process Tube

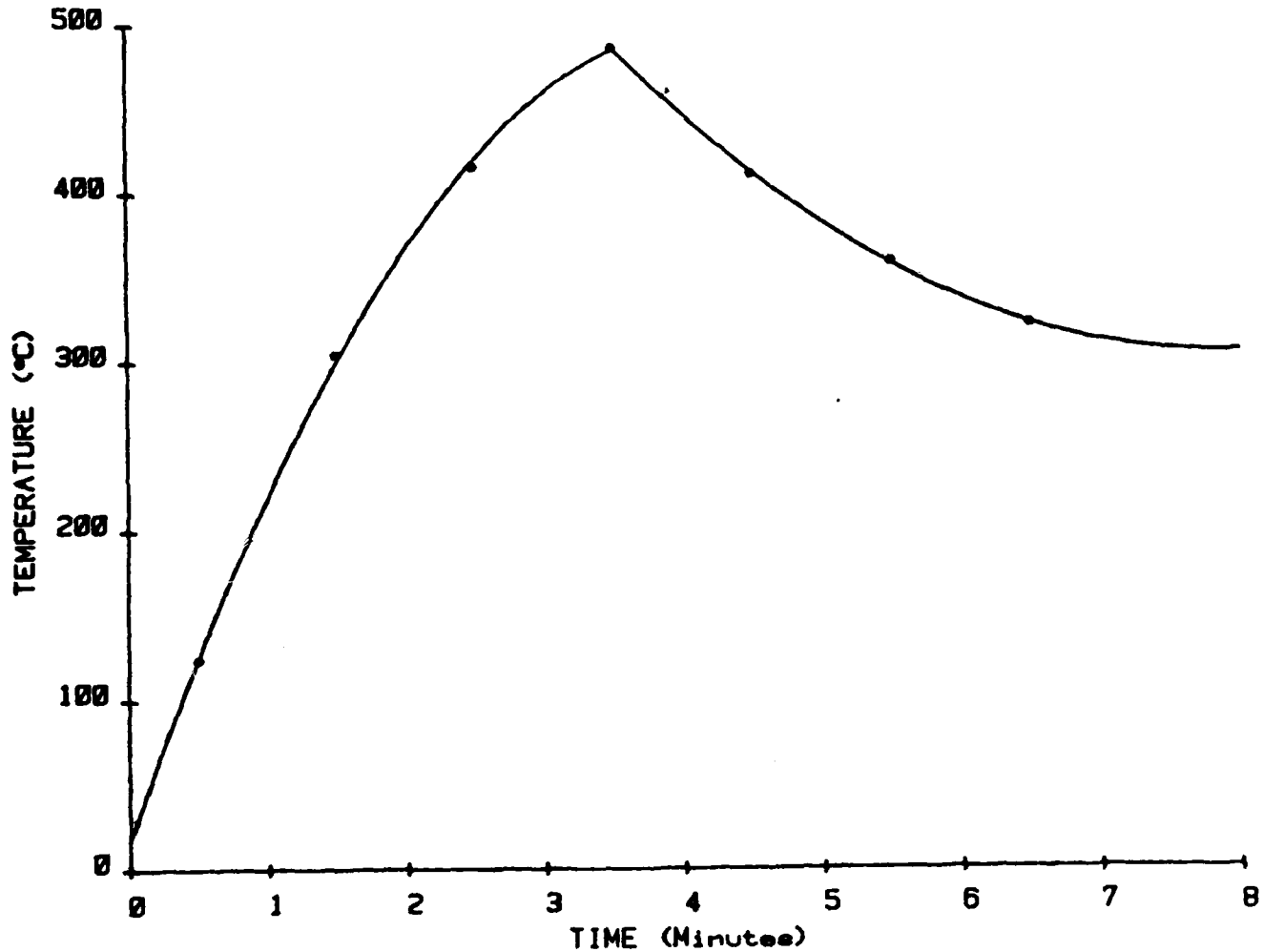

Figure A-3. Temperature Profile for Alloying Cycle

blowing a jet of forming gas directly at the boat when it sits in the capped end of the tube as shown in figure A-4.

After loading the top half of the wafer in the boat, the forming gas is allowed to flow through the tube from the rear end of the tube for 40 minutes in order to flush it, ensuring a moisture-free, oxygen-free environment for alloying. After the purging period, the boat is pushed into the alloying zone of the furnace. The temperature of the alloying cycle is closely monitored. When it reaches 485°C, the boat is withdrawn entirely from the furnace and is backed to the capped end of the tube. The forming gas is then turned on to flush the boat directly above the boat. The wafer is removed from the boat after the temperature of the boat is below 100°C.

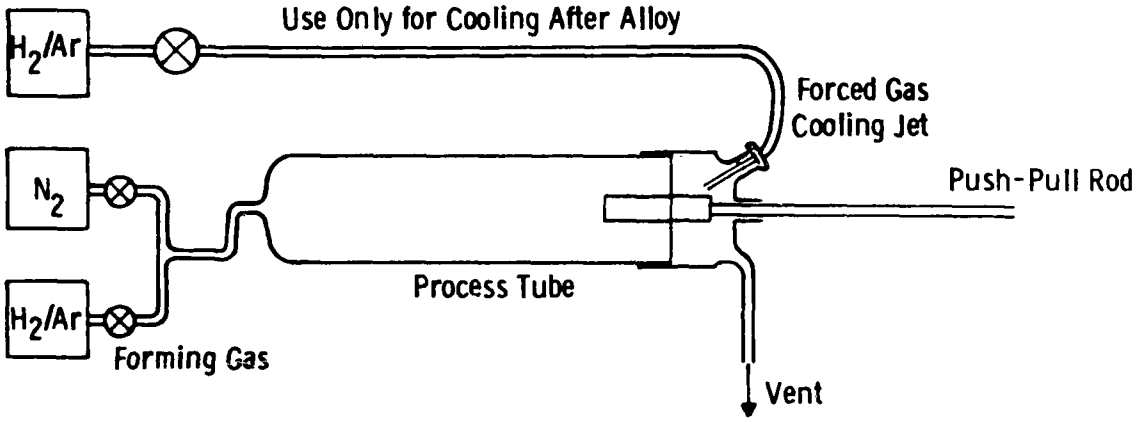

Figure A-4. Gas Flow System for Alloy Furnace

APPENDIX B

DRIFT MOBILITY PROFILE MEASUREMENTS EQUATION DERIVATION

The conductance of the active layer channel, Gc can be expressed as:

$$G_c = \frac{gw}{L} \int_{y_o}^{a} \mu_d (y)\, N(y)\, dy \qquad 1$$

where a is the active layer depth

$\mu_d(y)$ is the drift mobility, and

y_o is the depletion layer depth.

The total depletion layer charge under the gate is:

$$Q = qWL \int_{o}^{y_o} N(y)\, dy \qquad 2$$

The transconductance, g_m, is defined as:

$$g_m = \frac{\partial I_{DS}}{\partial V_g} = \frac{\partial G_c}{\partial V_g} \cdot V_{DS}$$

and the capacitance of the depletion layer is defined as:

$$C_g = \frac{-\partial Q}{\partial V_g}$$

From (1) and (2), the transconductance can be written as:

$$g_m = \frac{qw}{L} V_{ds} \left[\frac{\partial}{\partial V_g} \left(\int_{yo}^{g} \mu_d(y) N(y) dy \right) \right]$$

assume

$$\frac{dF(y)}{dy} = \mu_d(y) N(y)$$

then

$$\int_{yo}^{a} \mu_d (y)\, N(y)\, dy = \int_{yo}^{a} dF(y) = F(a) - F(yo)$$

$$\therefore gm = \frac{qw}{L} V_{DS} \left[\frac{\partial}{\partial V_{DS}} (F(a) - F(yo)) \right]$$

or

$$gm = \frac{qw}{L} \; V_{DS} \left[- \frac{\partial F(yo)}{\partial Vg} \right]$$

$$gm = \frac{qw}{L} \; V_{DS} \left[\frac{\partial F(yo)}{\partial yo} \left(- \frac{\partial yo}{\partial Vg} \right) \right]$$

or

$$gm = \frac{qw}{L} \; V_{DS} \left[\mu_d \; (yo) \; N(yo) \right] \left[- \frac{\partial yo}{\partial Vg} \right] \qquad 3$$

Similarly, the gate-source capacitance can be expressed as

$$Cg = qwl \left[- \frac{\partial}{\partial Vg} \left(\int_o^{yo} N(y) \; dy \right) \right]$$

assume

$$\frac{dG(y)}{dy} = N(y)$$

then

$$Cg = qwl \left[- \frac{\partial}{\partial Vg} \; (G(yo) - G(o) \right]$$

or

$$Cg = qWL \; N(yo) \; \frac{\partial y_o}{\partial V_g} \qquad 4$$

From the ratio of (3) and (4)

$$\frac{g_m}{C_g} = \frac{V_{DS}}{L^2} \; \mu_d \; (y_o)$$

the drift mobility can be written as:

$$\mu_d (y_o) = \frac{g_m \; L^2}{C_g \; V_{DS}} \qquad 5$$

MEASUREMENT AND DATA SMOOTHING PROGRAMS

MEASUREMENT 120 Measurements

1. Send Gate Voltage, V(I), [from V(0) to V(120)]
   From HP 6002 power supply [V_{min} V_{max}]

2. Read Gate Capacitance, C(I), from DVM
   Obtain C(0) → C(120)

3. Send Gate Voltage, V(I), starting from V_{min} to V_{max}
   from HP 6002 power supply

4. Read Drain Current, (M(I)),
   from DVM

DATA OBTAINED: V(I), C(I), M(I)

SMOOTH DATA

1. Smooth ((I) and MCI)

   C(I) = 1/2[C(I-2) + C(I+2)] + C(I+1) + C(I) + C(I-1)]/4

   M(I) = 1/2[M(I-2) + M(I+2)] + M(I+1) + M(I) + M(I-1) /4

2. Determine the range of data points which can be trusted
   L(1) to L(2)

FIT POLYNOMIAL

1. Use 5 points sectional fit

$\frac{1}{C_g^2} = Q_1 + Q_2 V_g + Q_3 V_g^2$ Quardratic fitting

2. Determine the depth, D(I) and concentration N(I)

$$D(I) = \frac{\epsilon\epsilon o}{A} \quad \frac{1}{C(I)}$$

$$N(J) = \frac{-2}{q\epsilon\epsilon oA^2} \Bigg/ \left[\frac{d\left(\frac{1}{C^2}\right)}{d\ V_g}\right]$$

EXTRAPOLATE TO SURFACE

(1) Find N(0)

Obtain data D(IO, N(I) from surface to L(2)

CALCULATE MOBILITY

1. Fit V(I), M(I) by Quardratic Eq.

$$M(I) = Q_1 + Q_2\ V(I) + Q_3\ (V(I))^2$$

from (5)

$$\mu_d\ (Vg) = \frac{g_m}{C_g}\ \frac{L^2}{V_{DS}}$$

$$\mu_d\ (Vg) = F(I) = \frac{\Delta I}{\Delta V} \quad \frac{L^2}{\frac{C(I) + C(I+1)}{2}} \cdot V_{DS}$$

$$F(I) = \frac{M(I) - M(I+1)}{V(I) - V(I+1)} \quad \left[\frac{2L^2}{C\ (I) + C(I+1)}\right]\left[\frac{1}{V_{DS}}\right]$$

APPENDIX C

SUBMICRON CONTACT MASK PROCUREMENT

In order to achieve reproducible power FETs for monolithic integrated amplifiers, it is necessary to maintain exacting control (±10 percent) over the submicron gates on the FET. Section 2.3 details the deep ultraviolet contact lithographic technology employed in the submicron gate fabrication. One limitation in the control of contact lithographic linewidth is determined by the mask used in the exposure. Contact masks used in the fabrication of nominal 1-μm FETs were generated using optical step and repeat equipment at Solid State Scientific[1]. However, the advent of submicron linewidth requirements has surpassed the capabilities of the optical pattern generation equipment.

To test the limits of optical pattern generation 1X master masks, a best effort 0.7-μm gate mask was manufactured at Solid State Scientific. Linewidths were measured on the 1X master mask and on FETs processed using this mask. Figure C-1 shows linewidth variation observed across a single FET on both the mask (±15 percent) and the processed gates (±19 percent). It is

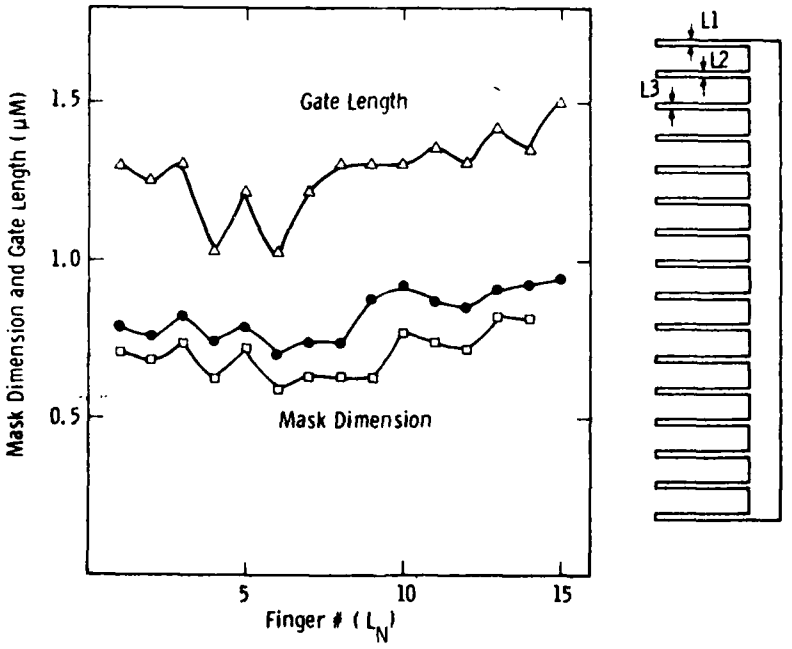

Figure C-1. Gate Length Variations on Devices and Optically - Generated Masks

important to note that the gate length changes observed in the contact mask were closely replicated in the processed FET. The optically generated submicron mask is clearly unuseable if the ±10 percent process variation requirements are to be maintained.

An alternative to optical mask generation is E-beam mask generation. Submicron gate masks are manufactured by Micro Mask[C2] by direct E-beam writing on 4 x 4-in. chromium coated quartz mask blanks. Figure C-2 compares nominal linewidth on multifinger gate FETs for optical and E-beam generated 1X master masks. The data indicates an average gate length across the 3-in. mask area of 0.76 μm ± 6 to -4 percent for the E-beam generated master mask. The optically generated 1X master demonstrated an average gate length of 0.81 μm +17 to -13 percent across the 3-in. mask area. Thus, to maintain ±10 percent gate tolerances in a submicron FET design, it is necessary to employ E-beam mask generation.

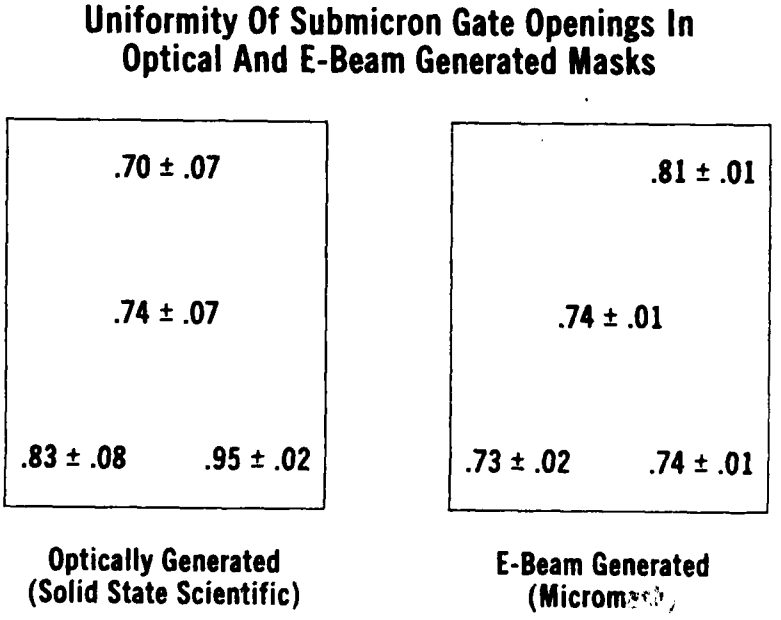

Figure C-2. Linewidths in Gate Mask

APPENDIX D

IRRADIATION OF GALLIUM ARSENIDE ICS, FET, AND SILICON DIOXIDE OVERLAY CAPACITORS

An initial experiment was conducted to determine the effect of high energy X-rays from a cobalt 60 source. Two two-stage amplifiers (IC32-C2-3 and IC32-B2-2), one 1200- μm periphery FET (IC32-B2-1E12B), and a silicon dioxide overlay capacitor (OLC2-1-B) with a 2500-A thick oxide were irradiated to a total dose of 5×10^6 rads. The results of the irradiation are shown in figures D-1, D-2, D-3 and D-4.

Amplifier IC32-B2-2 showed no change upon irradiation (figure D-1), while IC32-C2-3 showed a 2-dB lower gain after irradiation (figure D-2). The discrete device and the overlay capacitor showed no effects that could be attributed to the irradiation (figures D-3 and D-4).

Future experiments planned will include two additional conditions:

1. The temperatures of the devices will be closely monitored during the irradiation to ensure that degradation cannot be attributed to that variable. This is of particular importance when considering contact degradation.

2. The active devices will be biased during the irradiation. Recent data [D1] indicates that the most significant degradation of devices occurs under bias.

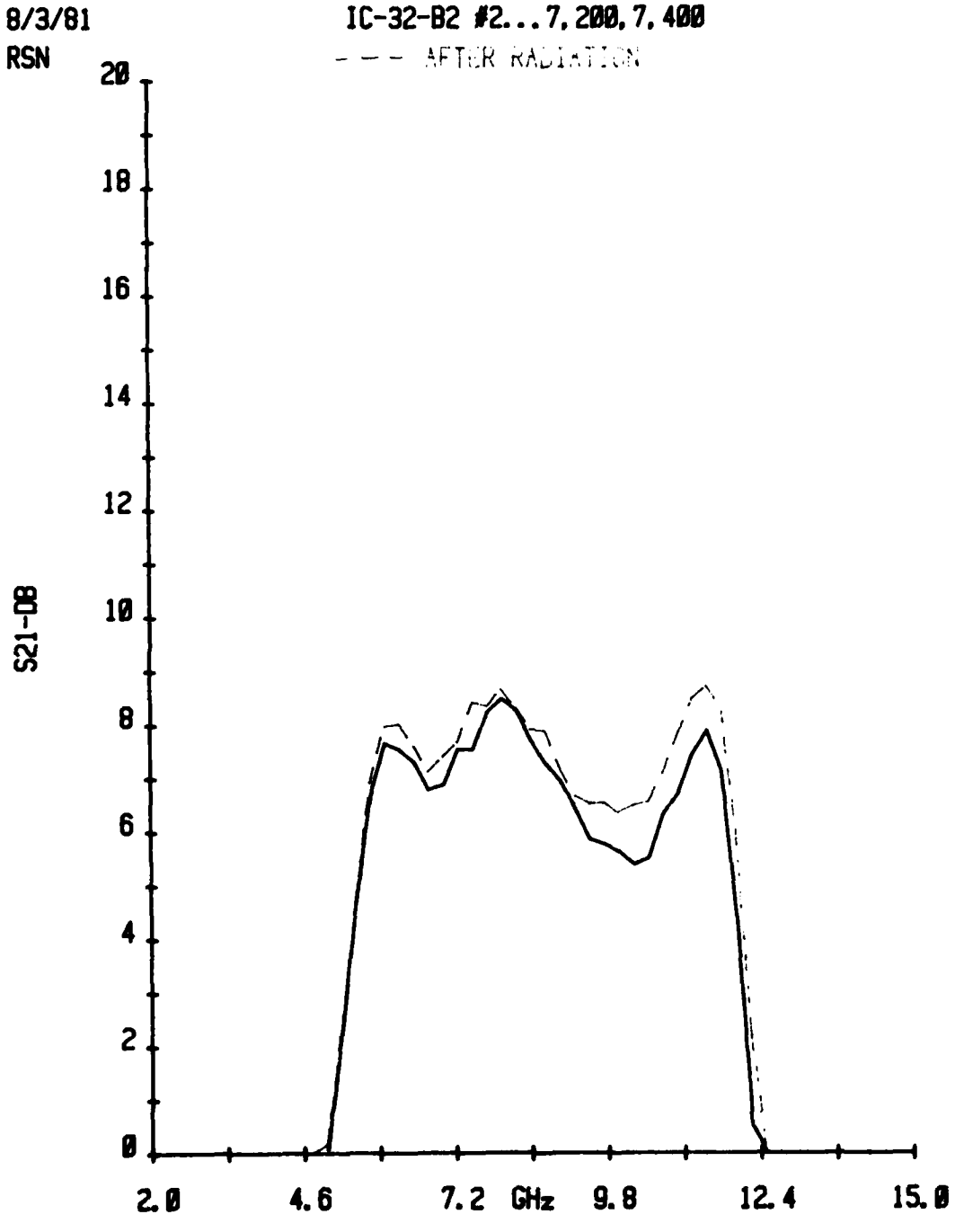

Figure D-1. Two-Stage Amplifier Gain Before and After Irradiation Showing No Degradation

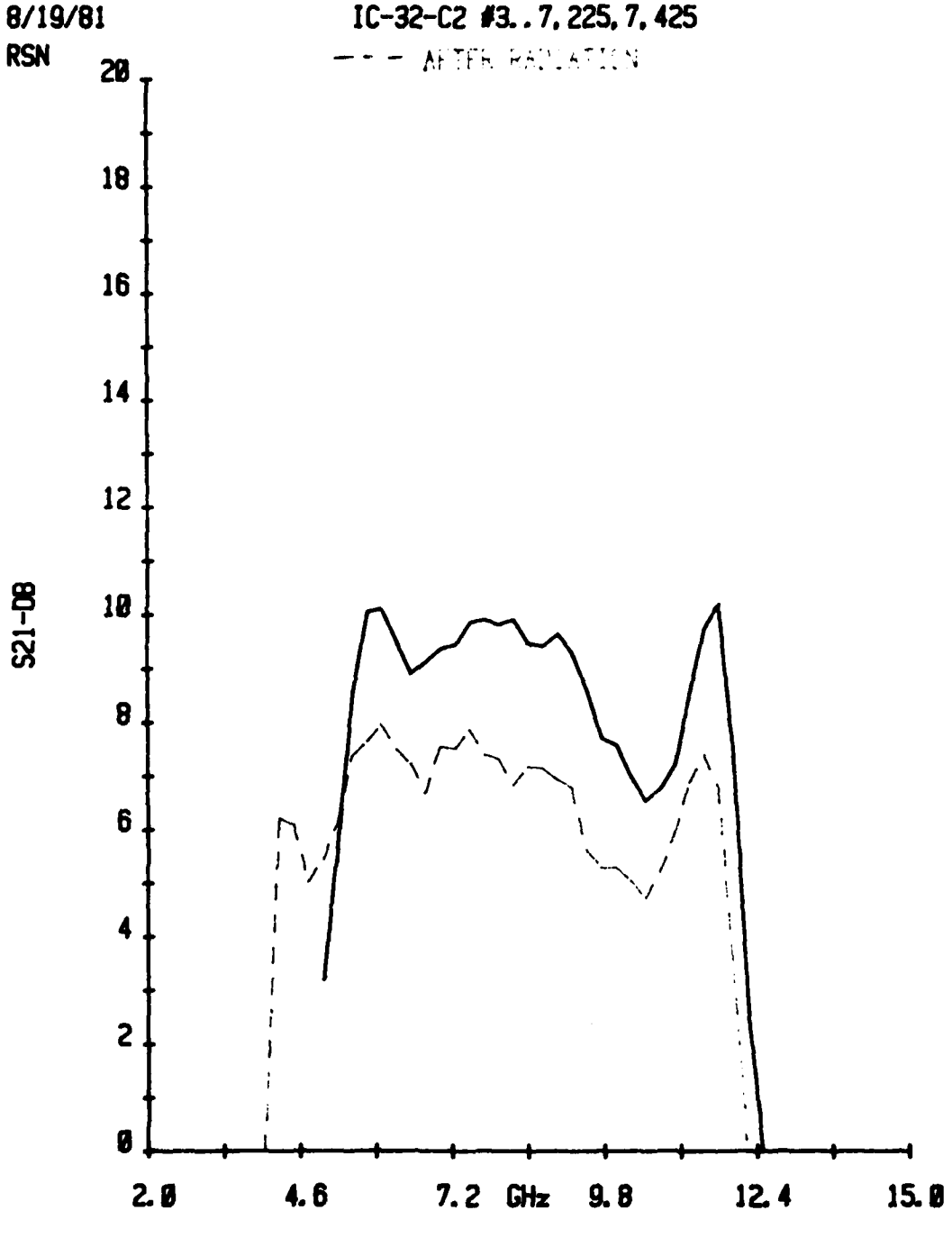

Figure D-2. Two-Stage Amplifier Gain Before and After Irradiation Showing 2-dB Degradation

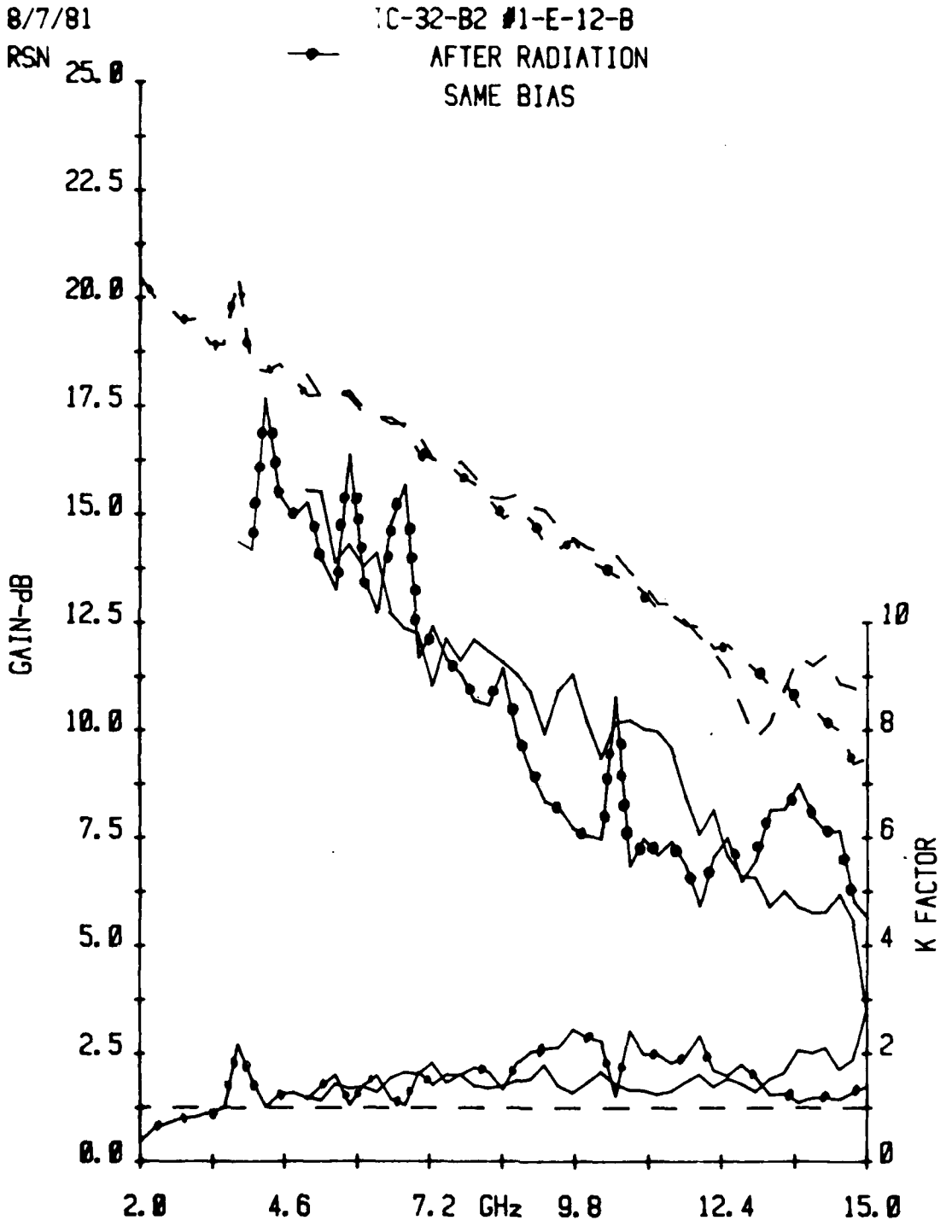

Figure D-3. Small Signal Gain of Discrete Device Before and After Irradiation

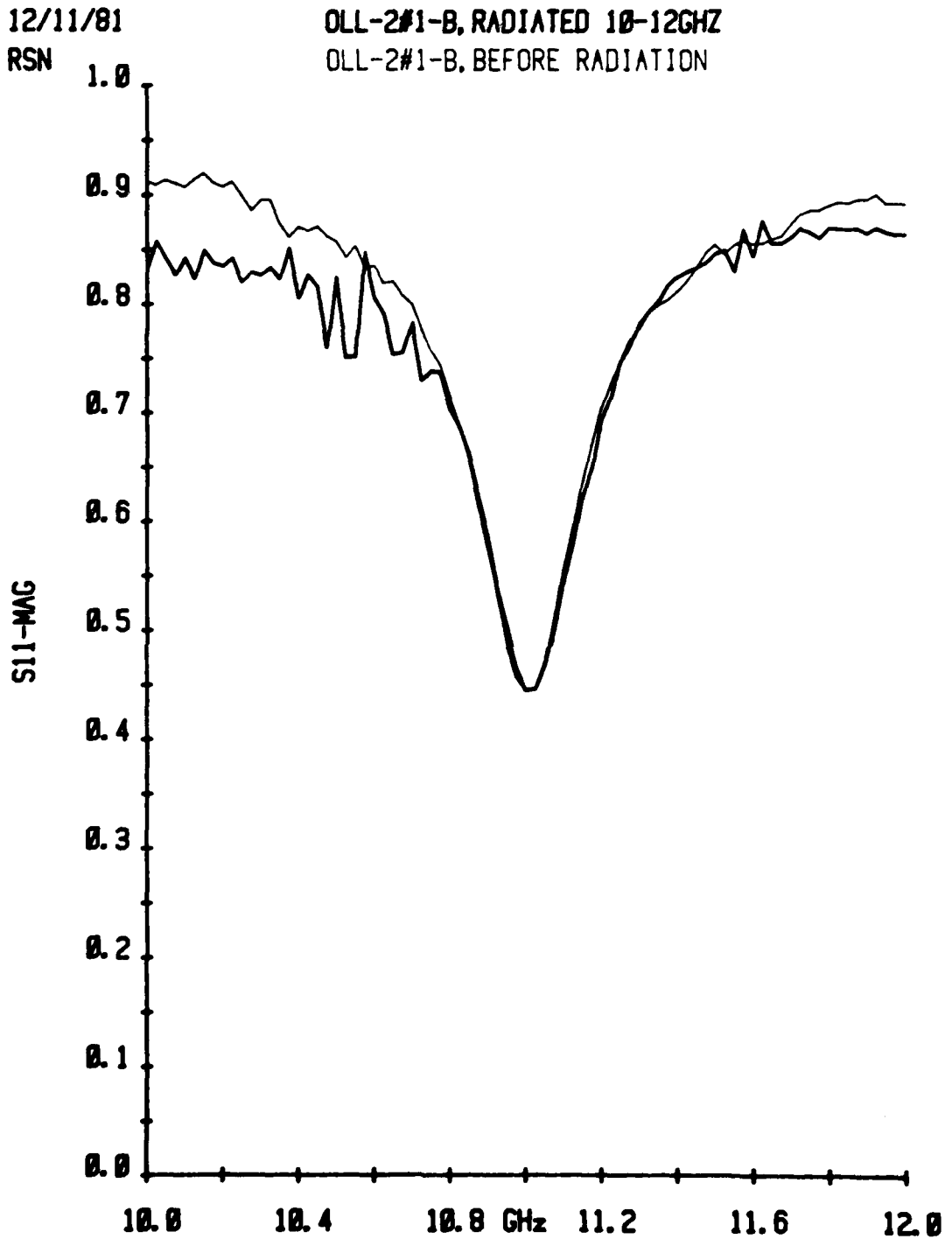

Figure D-4. S_{11} of Overlay Capacitor Before and After Irradiation

APPENDIX E

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